Wavesat

Chips for a new wireless world™

DM 256

Data Book

Document no. 256-59-01 (Draft L)

1375 autoroute Transcanadienne
Bureau 300
Dorval (Québec)
H9P 2W8 Canada

(514) 684-0200
Fax: (514) 684-0288

www.wavesat.com

DM 256

Data Book

Document no. 256-59-01 (Draft L)

Wavesat Wireless Inc.
1375 Trans Canada Highway, Suite 300
Dorval, Quebec
Canada, H9P 2W8
(888) 802-1616
(514) 684-0200
(514) 684-0288 (Fax)
www.wavesat.com
sales@wavesat.com
support@wavesat.com

This page has been left intentionally blank.

Publication History

The publication history is given in the table below.

Release	Owner	Date	Description
A-B	L.Law		
C	L.Law	May 14, 2004	
D	M.Lee	June 30, 2004	General format changes. Incorporation of the Programmer's Guide. Addition of the Figure and Table numbers, List of Definition and Terms.
E	M.Lee	July 30, 2004	General updates to document for information changes and corrections.
F	M.Lee	August 5, 2004	General updates and corrections. Addition of Pin Assignment Diagram, Correction for Register Description bit display conventions.
G	M.Lee	August 17, 2004	Addition of Mechanical and updated register information about the DM 256. More updates of the pin assignments. Updates to the look and feel of document's headers, general updates and corrections. Electrical Characteristics and power consumption updated. Added email contact information for Wavesat.
H	M.Lee	August 27, 2004	Updated ordering information, Section 5: Signal and Pin Descriptions, Frame parameters for setup using Frame Duration Codes 0-6. General updates to the look and feel of the document.
I	M.Lee	September 10, 2004	Updated Section 5: Signal and Pin Description. Clarification to the Section 3.5 on Data Transmission with the DM 256. Updated Section 6 Register Description for the Analog Control Register. Updated Register Address Table with missing Registers: Base ID, PDU & SNR. Clarification concerning section 3.3, the Frame Descriptor as Wavesat Proprietary format vs. IEEE 802.16 Standard.
J	M.Lee	September 24, 2004	Clarification of Prepended Header as a Statistical Header. Corrected DAC Register 1 Description. Update Range Offset to unsigned values. Moved the Frame Duration Codes to Section 3 from Section 4 to provide better clarity on Section 3. Provide detailed example of Frame Descriptor Configuration.
K	M.Lee	October 8, 2004	General updates and corrections to figures and tables. Performed another check on Section 5: Signal and Pin Description. Updated Signal Group Table pin counts and CPU Interface Signal Descriptions in Section 5. Updated Section 6 Register Address Table. Update Frame Descriptor Section with more details.
L	M.Lee	October 29, 2004	General updates and corrections from internal review. Section 3 Updates to Framing Parameters' Frame Duration Code: Sampling Frequency and corresponding symbols/frame., AGC and ALC Figures, updates to the Example Programming the Tx/Rx frame on the Subscriber and Base Stations. Section 6 Register Descriptions - Digital IF Register 1, 2. Updated Section 9 Thermal Resistance values, added new Drop-in Heat Spreader values. Updated Section 10 – Mechanical Specifications. Section 6, addition of Analog and Decoupling Specifications.

This page has been left intentionally blank.

About Wavesat

Wavesat, founded in 1993 and headquartered in Montreal, is a leading supplier of wireless chipsets for the Broadband Wireless Access (BWA) industry. As a technology leader in NLOS BWA solutions, (Non Line of Sight) Wavesat is partnering with equipment manufacturers and system integrators to deliver best-in-class 802.16 compliant broadband systems based on the most advanced COFDM (Coded Orthogonal Frequency Division Multiplexing) developments.

The Wavesat offer includes a full suite of building blocks (including PHY, MAC hardware, processors, DACs, ADCs and other integrated elements) to build a wide range of distinctive and cost-effective BWA products, from highly efficient base stations to low power mobile CPE (Customer Premise Equipment).

The Wavesat technology is user friendly, easy to integrate and enables superior infrastructure and communication performances at lower cost than proprietary based solutions.

Wavesat leadership

At its asset and at the industry's benefit, Wavesat is the first in the industry to introduce an IEEE 802.16- 2004 compliant PHY chipset with forward compatibility to 802.16e standard for mobile applications.

As a premier communications integrated circuit provider, Wavesat has unparalleled ability to offer BWA system design solutions, which are supported by user friendly development system, comprehensive reference designs and resourceful talented field engineering teams. All these valuable design tools, customer support services and engineering competencies are available to Wavesat system partners.

Wavesat, a skilled and dedicated team

Wavesat's dynamic and diverse team of scientists and engineers is entirely committed to delivering the highest quality and most cost-effective broadband wireless products available on the market. This dedication and passion has resulted in Wavesat producing innovative wireless solutions which push the boundary on what is currently possible. In many ways, the Wavesat R&D team is a "think tank" for wireless developments, especially in the leading edge field of OFDM technology.

Wavesat, more than 10 years of commitment to the wireless industry

The company has built a solid background and reputation in delivering baseband, IF and RF subsystems for the wireless industry. Wavesat now dedicates all its engineering and marketing resources to the IEEE standard based BWA industry as a fabless BWA semiconductor company.

Wavesat Wireless Inc.

1375 Trans Canada Highway, Suite 300

Dorval, Quebec

Canada, H9P 2W8

(888) 802-1616

(514) 684-0200

(514) 684-0288 (Fax)

www.wavesat.com

support@wavesat.com

sales@wavesat.com

This page has been left intentionally blank.

List of Sections

This page has been left intentionally blank.

Table of Contents

List of Tables

List of Figures

Section: 1 Introduction

1.1 Product Description

The DM 256 integrated circuit implements the IEEE P802.16-2004 Wireless MAN-OFDM™ PHY layer protocol and is designed to be the main component of an Orthogonal Frequency Division Multiplexing (OFDM) modem for Broadband Wireless Access (BWA). The PHY has two complementary functions. One is to process data for transmission where the output is a Baseband In phase / Quadrature (I/Q) signal or a programmable IF signal. The process is reversed for the second function of receiving data where the input is a Baseband I/Q signal or a programmable IF signal. For data reception, the PHY implements proprietary synchronization and channel equalization methods for OFDM. Synchronization includes frequency synchronization as well as timing synchronization.

1.2 Highlights

- Forward compatibility with IEEE 802.16e PHY for mobile applications.
- Industry leading 5 bits/sec/Hertz spectral efficiency.
- Meets all six SUI (Stanford University Interim) Non Line of Sight (NLOS) channel models.
- Supports TDD (Time-Division Duplexing), HFDD (Half-Duplex Frequency Duplexing) and FDD (Frequency-Division Duplexing).
- IEEE 802.16- 2004 compliant PHY Integrated Circuit using Wavesat patented algorithms.

1.3 Features

- 208 pin PQFP (Plastic Quad Flat Pack).
- OFDM (Orthogonal Frequency Division Multiplexing) upstream and downstream.
- 256 point FFT (Fast Fourier Transform).
- Concatenated Reed-Solomon/Viterbi.
- Programmable Guard Intervals.
- Digital IF: Digital or analog programmable IF or analog IQ interface with programmable Bandwidths.

1.4 Benefits

- Integrated analog front end for simplified board design.
- AGC, AFC and Tx Gain control outputs for simple interfacing to RF circuitry.
- Low cost.
- Low power consumption.
- Same chip can be used for Base Station as well as for Customer Premise Equipment (CPE).

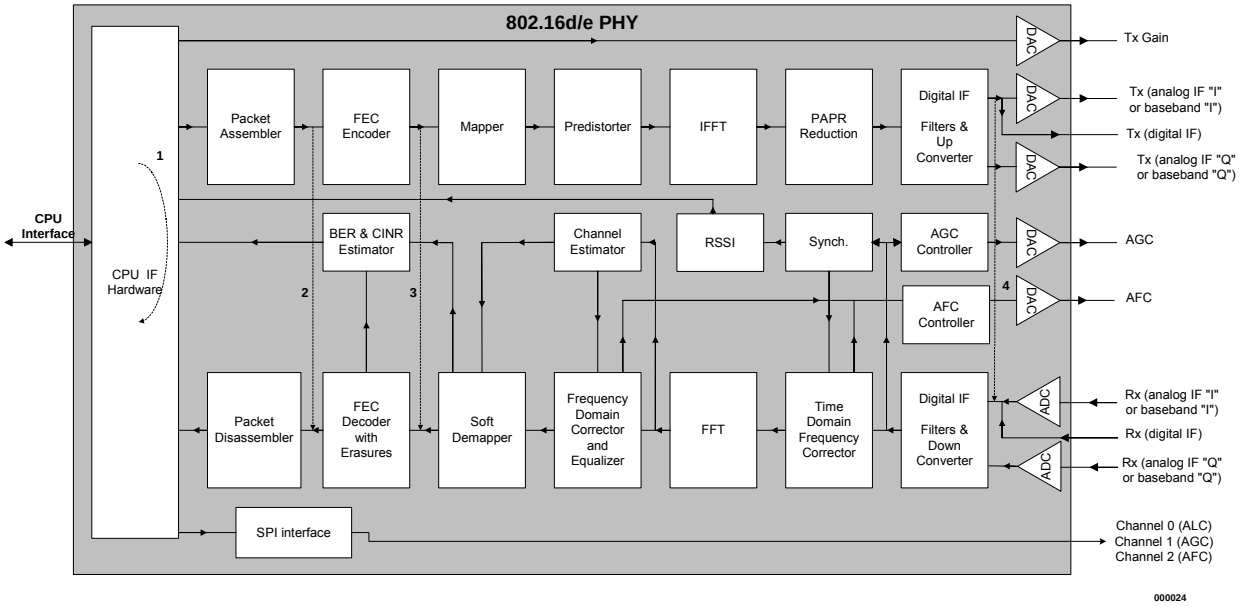


Figure 1: DM 256 Block diagram

Section: 2 Characteristics

2.1 General Specifications

Table 1: General Specifications of the DM 256

Frequency band	2 to 11 GHz
Bandwidths	• 1.75 MHz • 3.5 MHz • 7 MHz • 10 MHz
Spectral Efficiency	5 b/Hz-sec (uncoded at 64 QAM)
Modulation	OFDM (4/16/64 QAM, BPSK) upstream and downstream
Topology	Point-to-multipoint
Multiplexing Techniques	• Time Division Multiplexing (TDM) downlink • Time Division Multiple Access (TDMA) uplink
Duplexing Methods	• Frequency Division Duplexing (FDD) • Half-Duplex Frequency Division Duplexing (H-FDD) • Time Division Duplexing (TDD)
Frame Sizes	Programmable (5, 10, 20 ms)
Channel Coding	• Randomization • Concatenated Reed-Solomon/Viterbi • Interleaving
FFT Size	256 points
Guard Intervals	Programmable (1/4, 1/8, 1/16, 1/32)
Transceiver Interface	Digital and Analog IF and Analog IQ
Power Input	• 3.3V • 1.8V
Power Consumption	• 3.3 V I/O = 95.8 mW • 1.8 V core = 505 mW • 3.3 V analog = 302.8 mW • Total Power = 0.9 W
Package	• 208-pin Plastic Quad Flat Pack (PQFP)

2.2 ADC/DAC Specifications

Table 2: ADC/DAC Specifications of the DM 256

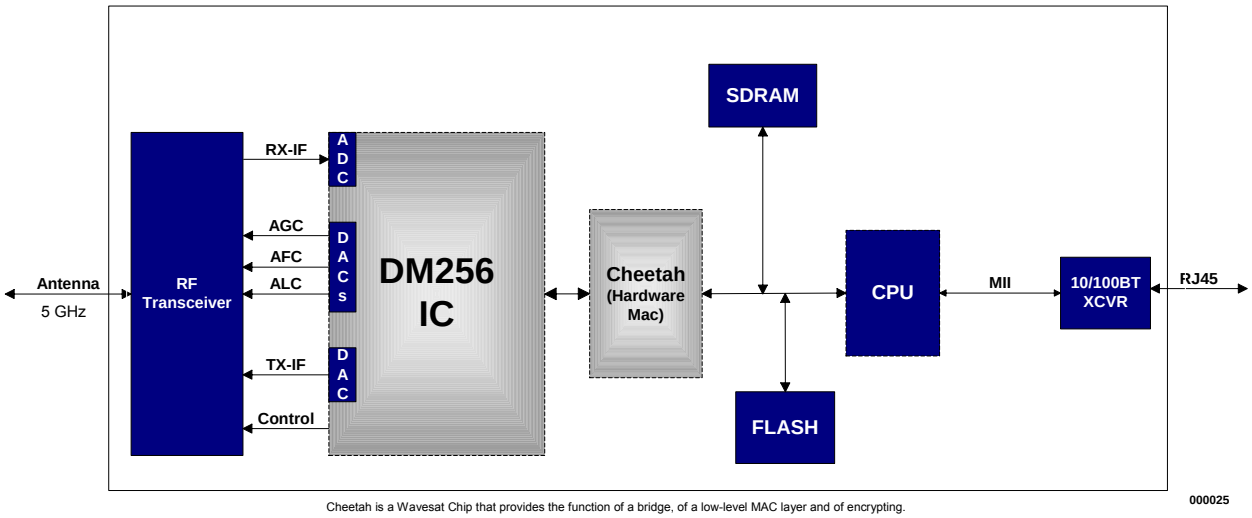
Resolution	10 bits
Sampling Rate	> 44 MS/s
Conversion Rate	50 MHz
Analog Input	2 Vpp
Analog Output	2 Vpp
Analog Supply Voltage	3.3 V ±10%
Digital Supply Voltage	1.8 V ±10%
Offset Error	-2% FS (min); +2% (max)
Gain Error	-5% FS (min); +5% (max)
Gain Matching	-1% FS (min); +1% (max)
Offset Matching	TBD
Differential Non-linearity	±0.5 LSB
Integral Non-linearity	±1 LSB

2.3 Radio Requirements

Table 3: Radio Requirements of the DM 256

BS Tx Frequency Accuracy	• ±4 ppm
Phase Noise	• ≤ -90 dBc/Hz at 10 kHz from the carrier
Power Amplifier Linearity (P1dB)	• Back-off from P1dB point ≥ 8 dB
I/Q Imbalance	• Gain imbalance ≤ 0.7 dB • Phase imbalance ≤ 4 degrees

2.4 Modem Reference Design



Cheetah is a Wavesat Chip that provides the function of a bridge, of a low-level MAC layer and of encrypting.

Figure 2: Modem Reference Design

This page has been left intentionally blank.

Section: 3 Functional Descriptions

3.1 OFDM Frame

DM 256 is based on Orthogonal Frequency Division Multiplexing (OFDM) frame transmission. An OFDM frame contains a downlink (DL) sub-frame and an uplink (UL) sub-frame.

Time-Division Duplexing (TDD):

- The DL sub-frame occurs first, followed by the UL sub-frame. See Figure 3: TDD Mode.

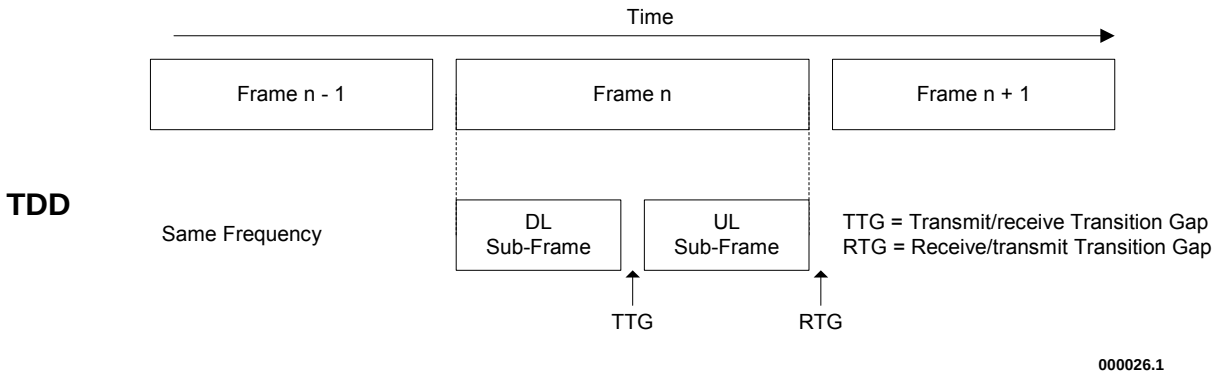


Figure 3: TDD Mode

Frequency-Division Duplexing (FDD):

- Both UL and DL transmissions occur simultaneously on different frequencies. See Figure 4: FDD Mode.

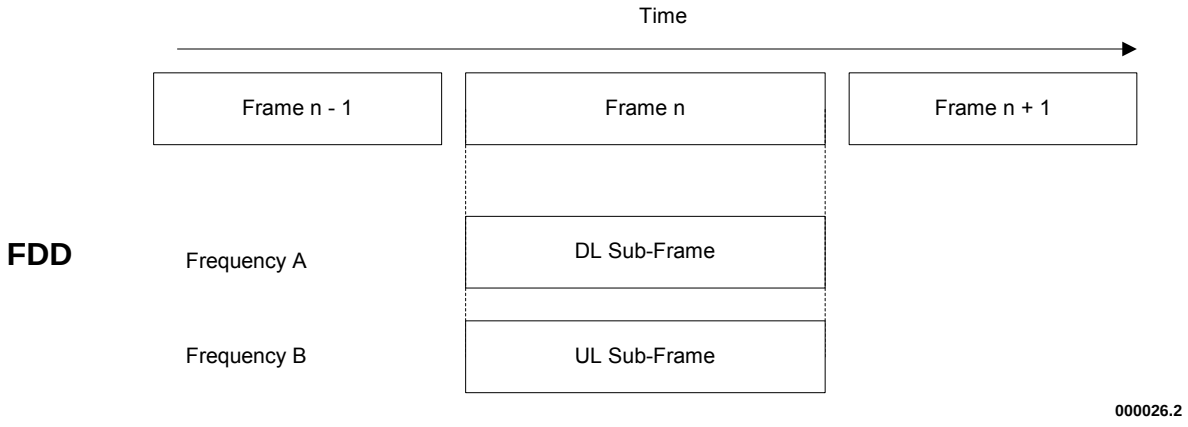


Figure 4: FDD Mode

Half-Duplex Frequency Division Duplexing (H-FDD):

- The transmissions occur at different times and on different frequencies. See Figure 5: H-FDD Mode.

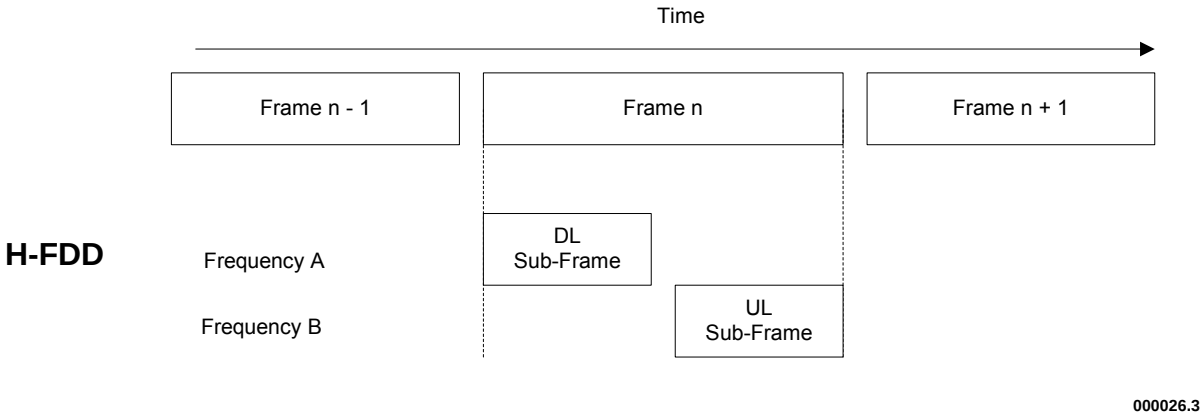


Figure 5: H-FDD Mode

3.2 Frame Structure

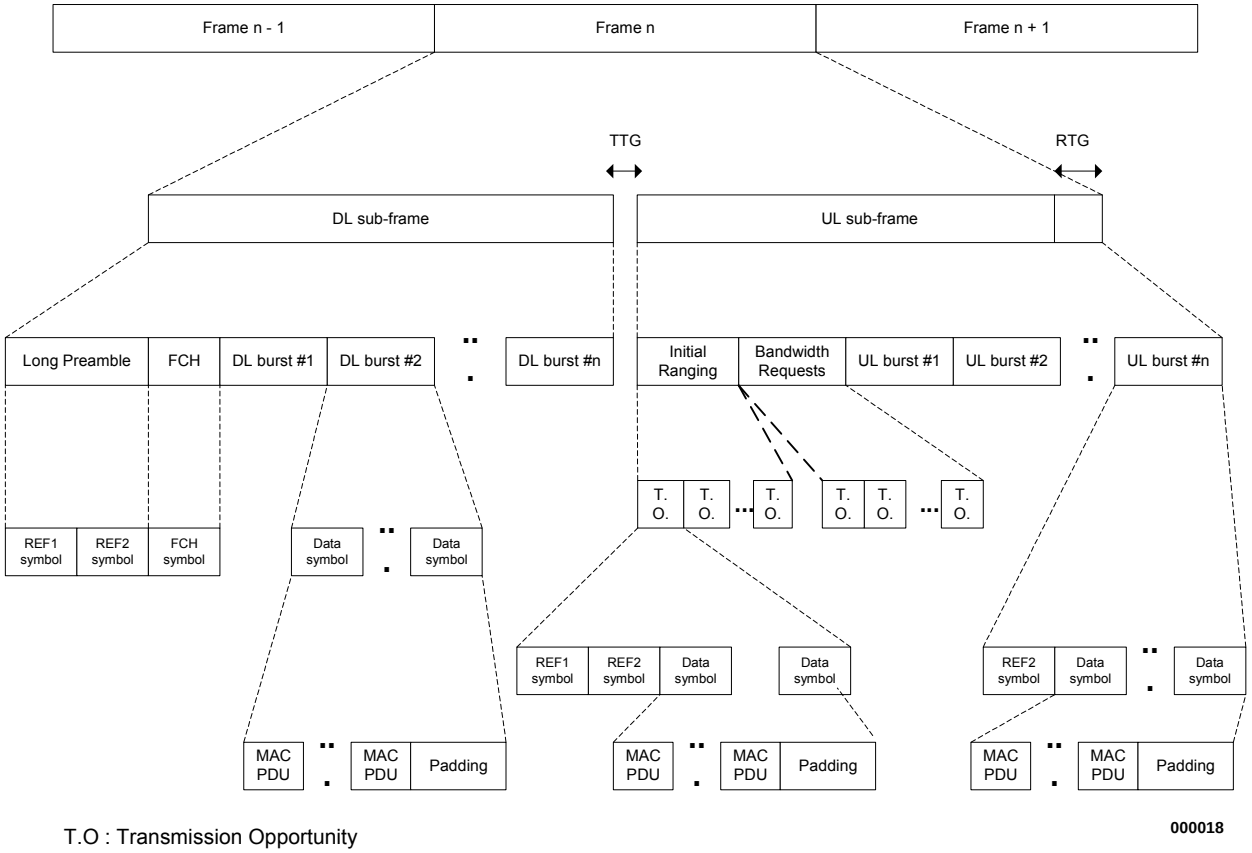
A DL sub-frame consists of the following slots:

Long preamble.
Frame Control Header (FCH).
DL (Downlink) bursts.
Intended gaps TTG/RTG (Transmit/Receive Transition Gap/Receive/Transmit Transition Gap).

A UL sub-frame consists of the following slots:

Transmission Opportunities (Contention Slots) for initial ranging and bandwidth requests.
UL bursts.

To describe the frame configuration, each of these bursts can be represented by one or more symbols as shown in Figure 6: OFDM Frame Structure for a TDD System, Table 4: Symbol Definitions and Table 5: Elements in an OFDM Frame.



T.O : Transmission Opportunity

Figure 6: OFDM Frame Structure for a TDD System

3.2.1 Symbol Definitions

Table 4: Symbol Definitions defines the symbols used by the DM 256 in a Frame Descriptor to define an OFDM frame and Table 5: Elements in an OFDM Frame describes the elements within the OFDM frame.

Table 4: Symbol Definitions

Symbol	Description
REF1	The REF1 symbol defines the first half of the long preamble. It is composed of 4 repetitions of a 64-sample fragment, preceded by a CP.
REF2	The REF2 symbol constitutes the second half of the long preamble. The REF2 symbol is composed of 2 repetitions of a 128-sample fragment, preceded by a CP. When REF2 symbol is not preceded by the REF1 symbol, it represents the short preamble.
FCH	The FCH symbol is used to create the FCH burst.
Data	A Data symbol specifies modulation and coding rate to be applied to OFDM symbols carrying payload data.
Midamble	A Midamble is composed of 2 repetitions of a 128-sample fragment, preceded by a CP.
Channel Measurement Gap (CMG)	A CM GAP symbol is used to instruct the DM 256 to perform a channel measurement.

Table 5: Elements in an OFDM Frame

Elements	Description
Long Preamble	The Long Preamble is defined as a REF1 symbol followed by a REF2 symbol. The long preamble is transmitted by the Base Station at the beginning of a frame and by a Subscriber Station during initial ranging or bandwidth request.
Short Preamble	The Short Preamble is defined as the REF2 symbol.
FCH	The FCH burst is specified as an FCH symbol.
DL bursts	Each DL burst is represented by Data symbols having the same modulation and coding rate.
Transmission Opportunities	A number of transmission opportunities (contention slots) maybe reserved in the UL sub-frame for initial ranging and bandwidth requests by Subscriber Stations. To use a transmission opportunity, a Subscriber Station must transmit a Long Preamble (REF1 and REF2) as well as the required number of Data symbols.
UL bursts	A UL burst begins with either the Short or Long Preamble followed by Data symbols.
Gap	A Gap is an interval in time during which no data is transmitted.

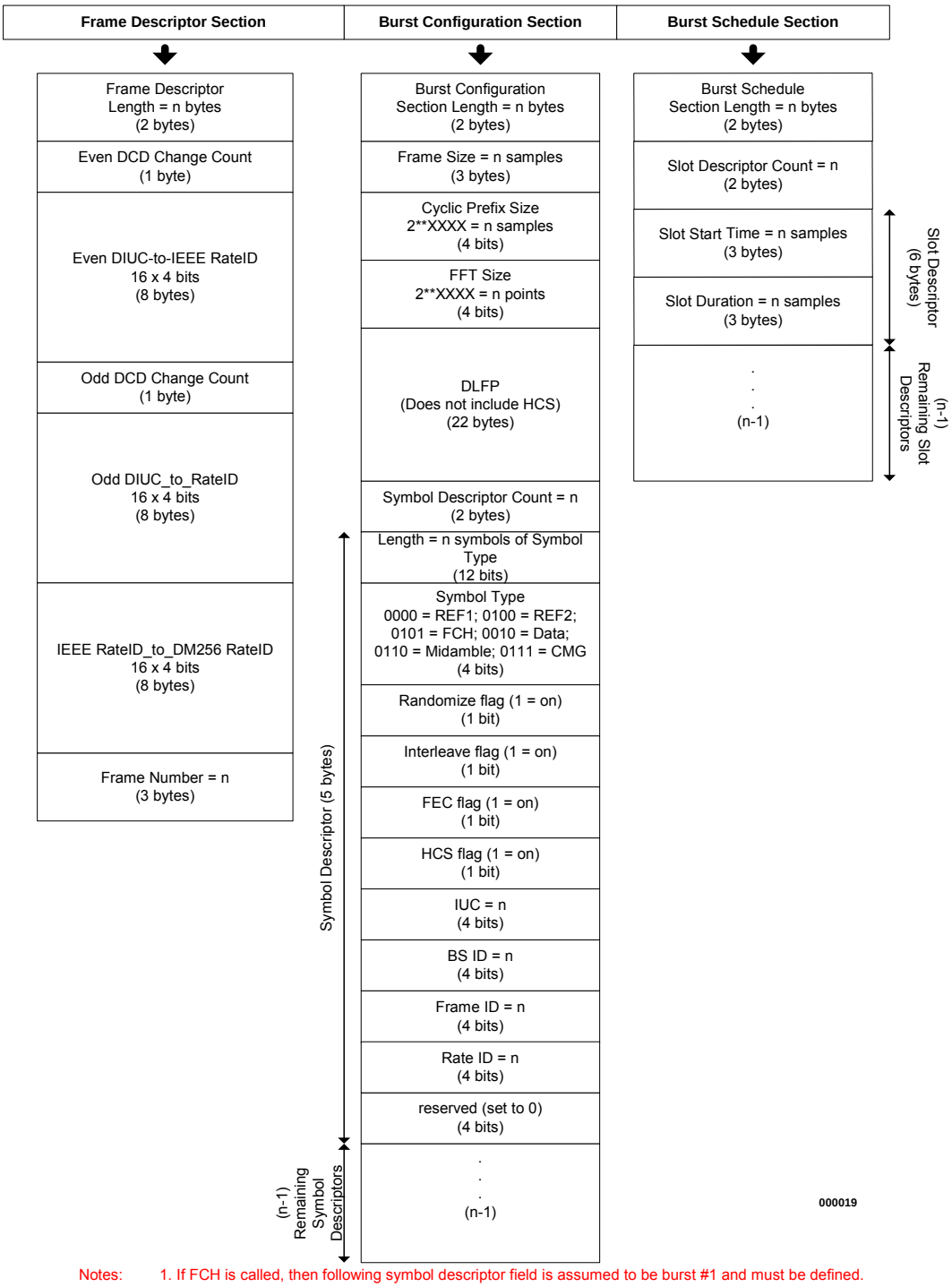
3.3 Frame Descriptor

In DM 256, the frame configuration is specified in the form of a Frame Descriptor. The Frame Descriptor is divided into three sections as follows:

Frame Descriptor Section.
Burst Configuration Section.
Burst Schedule Section.

Note	The Frame Descriptor described in this document is a Wavesat Proprietary format.

The content of each of the sections is outlined in Figure 7: Structure of the Frame Descriptor and is described in more details in Table 6: Frame Descriptor Section Elements, Table 7: Burst Configuration Section Elements and Table 8: Burst Schedule Section Elements.



Notes:
1. If FCH is called, then following symbol descriptor field is assumed to be burst #1 and must be defined.
2. The FCH burst is always transmitted using the default DM256 Rate ID. The contents of DLFP is copied by DM 256 into the FCH Burst.
3. OFDM Frame number acts as a continuity counter with a modulous of Superframe Size.
4. Reserved field should be initialized with 0
5. Symbol Descriptor uses DM 256 Rate ID.
6. Only the indicated symbol types may be used.
7. This frame descriptor is a Wavesat Proprietary Format.

Figure 7: Structure of the Frame Descriptor

Table 6: Frame Descriptor Section Elements

Frame Descriptor Section Elements	Description
Frame Descriptor Length	Indicates the number of bytes following in the Frame Descriptor.
Even DCD Change Count	Most recent Even valued DCD Change Count.
Even DIUC to IEEE Rate ID	Corresponding Even DIUC to IEEE Rate ID conversion table.
Odd DCD Change Count	Most recent Odd valued DCD Change Count.
Odd DIUC to IEEE Rate ID	Corresponding Odd DIUC to IEEE Rate ID conversion table IEEE.
Rate ID to DM 256 Rate ID	IEEE Rate ID to DM 256 Rate ID conversion table.
Frame Number	The OFDM Frame Number specifies the Frame in which the Frame Descriptor applies. Burst Configuration Section.

Table 7: Burst Configuration Section Elements

.Burst Configuration Section Elements	Description
Burst Configuration Section Length	Indicates the number of bytes following in the Burst Configuration Section.
Frame Size	Indicates the frame size in complex sample count. This value is a function of the frame duration, cyclic prefix, carrier frequency and bandwidth.
Cyclic Prefix (CP) Size, n	Indicates the Cyclic Prefix Size in complex samples, where samples = 2^n. Valid values for n = 3, 4, 5, 6.
Fast Fourier Transform (FFT) Size, n	Indicates the size of the FFT where size = 2^n. Valid values for n is 8.
DLFP	IEEE 802.16 Downlink Frame Prefix.
Symbol Descriptor Count	Indicates the number of Symbol Descriptors in the Frame Descriptor.
Length	Indicates the number of symbols in the Symbol Descriptor.
Symbol Type	Indicates the type of symbol in the Symbol Descriptor.
Randomize Flag	When this flag is set to 1, the randomization is performed on the uncoded data block. When the flag is set to 0, no randomization is performed.
Interleave Flag	When this flag is set to 1, the interleaving is performed on the uncoded data block. When the flag is set to 0, no interleaving is performed.
FEC Flag	When this flag is set to 1, the Forward Error Correction (FEC) is enabled. When the flag is set to 0, the FEC is disabled.
HCS Flag	When this flag is set to 1, the HCS is computed for the FCH burst. When the flag is set to 0, the HCS is not computed.
IUC	The Interval Usage Code (IUC) is used in conjunction with the Frame ID and Base Station ID fields to perform randomization for each burst.
BS ID	The Least Significant four bits of the Base Station ID.
Frame ID	The Least Significant four bits of the current Frame Number.
Rate ID	Indicates the type of modulation used by the burst.

CP Size	Samples 2^n
1/4	2^6
1/8	2^5
1/16	2^4
1/32	2^3

Table 8: Burst Schedule Section Elements

Burst Schedule Elements Section	Description
Burst Schedule Section Length	Indicates the number of bytes following in the Burst Schedule Section.
Slot Descriptor Count	Indicates the number of Slot Descriptors in the Frame Descriptor. A Slot Descriptor is required for each Symbol Descriptor.
Slot Start Time	Indicates, in sample counts, the slot start time relative to the start of the frame.
Slot Duration	Indicates the slot duration in sample counts.

3.4 Frame Configuration Parameters

3.4.1 Symbol Configurations

Table 9: Symbol Configurations lists the symbols that can be transmitted in a frame and shows the configuration required for each symbol in the Frame Descriptor.

Table 9: Symbol Configurations

Parameters / symbol	REF1	REF2	FCH	Data	Midamble	CMG
Bit Configuration	0000	0100	0101	0010	0110	0111
Randomize	0	0	1	1	0	0
Interleave	0	0	1	1	0	0
FEC	0	0	1	1	0	0
CRC	0	0	0	0	0	0
IUC (DIUC/UIUC)	0	0	0	0	0	0
Rate ID	0	0	0-6	User-defined	0	0

3.4.2 DM 256 Rate ID

DM 256 supports the following rate ID, see Table 10: DM 256 Rate ID for details.

Table 10: DM 256 Rate ID

DM 256 Rate ID	Modulation and Coding Scheme
0	QPSK (RS+CC) 1/2
1	QPSK (RS+CC) 3/4
2	16-QAM (RS+CC) 1/2
3	16-QAM (RS+CC) 3/4
4	64-QAM (RS+CC) 2/3
5	64-QAM (RS+CC) 3/4
6	BPSK (CC) 1/2

3.4.3 Cyclic Prefix

The Cyclic Prefix (CP) Size must be specified as part of the frame configuration. The length of each symbol is a function of the CP Size as shown in. Table 11: Symbol Length for Each CP Size See Table 12: CP Size Example for an example.

Table 11: Symbol Length for Each CP Size

Cycle Prefix (CP) Size	Symbol Length (Complex Samples)
1/32	264
1/16	272
1/8	288
1/4	320

Table 12: CP Size Example

For Example	Description
CP size	1/16
Number of complex samples per symbol length	272
A burst containing 5 symbols starts	2720
Its duration must then be set	1360
Next symbol must start	4080

3.5 Data Transmission with the DM 256

Transmission with the DM 256 OFDM is driven primarily by the two Tx Frame Descriptor Buffers.

The basic principle is each Tx Frame Descriptor must indicate: how the DM 256 should encode and modulate a stream of bytes that is placed in the Tx FIFO on a frame-by-frame basis. The purpose of having two descriptors is that: while the DM 256 is processing one descriptor (say Tx Frame Descriptor 1) and transmitting the data for Frame n, the MAC is constructing the descriptor (Tx Frame Descriptor 2) and preparing the data for Frame n + 1. In effect, there is a toggling from one Tx Frame Descriptor to the other as the DM 256 transitions from Frame to Frame.

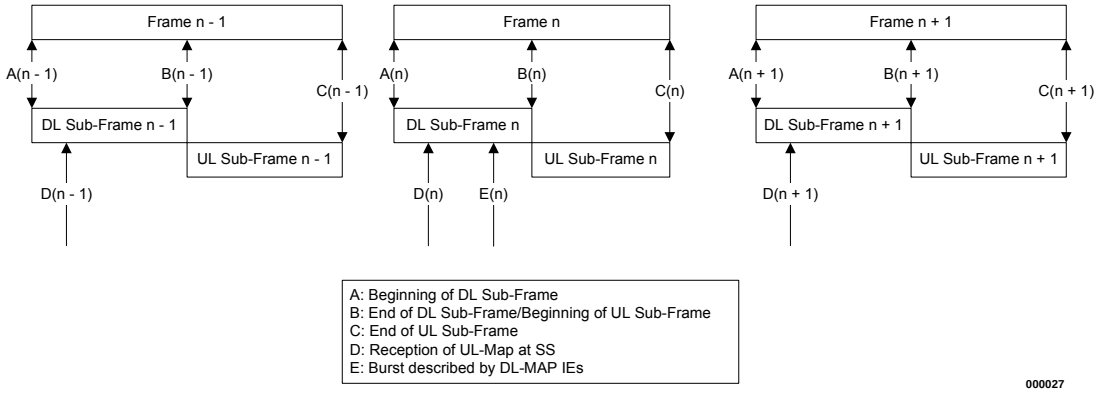


Figure 8: TDD Framing

For any given Frame ***n***, transmission is a four-step process that must meet specific timing requirements:

1. When **scheduling**, the MAC Layer must decide how much bandwidth is allocated to each CID (Connection Identifier) and the order the data is to be transmitted.

   The algorithm used to decide scheduling is not defined by the DM 256 and is implementation specific.

2. ***Transfer of the data stream to the DM 256***: several methods are available for transferring the data scheduled in Step 1 from the MAC memory space to the DM 256 Tx FIFO.

   The DM 256 expects the data for a given Frame to be available in the Tx FIFO at the moment that the data is to be transmitted. While the DM 256's Tx FIFO is 4 KB, a single Tx data stream may exceed this size. If at the moment of symbol construction, there is insufficient data in the Tx FIFO, the DM 256 will transmit a symbol in which the uncoded data consists of the byte value 0xFF to maintain Frame synchronization. As a result, the data is now desynchronized with the Tx Frame Descriptor with each unused byte remaining in the Tx FIFO at the end of the Frame. Consequently, the data transfer rate from the MAC Layer to the Tx FIFO must be meet or exceed the data "consumption" rate of the DM 256.

   The maximum data throughput on transmission occurs under the following parameters:

   Channel Bandwidth = 10 MHz.

   Coding = QAM 64 ¾

   CP = 1/32

   Frame Duration Code = 6 (20 msec or 50 frames/sec)

   [865 symbols/frame - 3 overhead symbols/frame]= 862 symbols for single burst

   Where 3 overhead symbols/frame = (Long preamble (2) + FCH (1))

   FDD = ((862 * 144 coded block size bytes for QAM 64*(¾coding rate)) -1 Viterbi tail byte per frame) *8 bits/byte*50 frames/sec

   = 37.238 x 10^6 bits/sec

Notes	When the D/A sampling clock for the DM 256 is 40 MHz , the Baseband sampling rate for the 10 MHz channelization is Fs=11.43 MHz, which is not the rate specified in the P802.16-Revd/D5 standard. To meet that requirement the D/A sampling (and the A/D sampling clock) needs to be set to 40.32 MHz. The software provided with the Development Kit assumes, however Fs=11.43 MHz, when specifying the number of symbols allowed per frame duration. When 40.32 MHz sampling clock is used, this results in a change to 872 symbols/frame

3. ***Construction of a Tx Frame Descriptor***: the Tx Frame Descriptor indicates how the DM 256 should process the data bytes based on the scheduling decisions made in Step 1

4. ***Transfer and Activation of the Tx Frame Descriptor to the DM 256***: several methods are available for writing the Tx Frame Descriptor to the DM 256.

   Setting it to 'Ready' allows the DM 256 to read its contents and fetch the corresponding data at the appropriate frame time. The DM 256 will fragment the MAC PDU(s) in its Tx FIFO into uncoded data blocks whose sizes are based on the modulation and coding type. It will then randomize, encode, and interleave the uncoded blocks into OFDM Symbols.

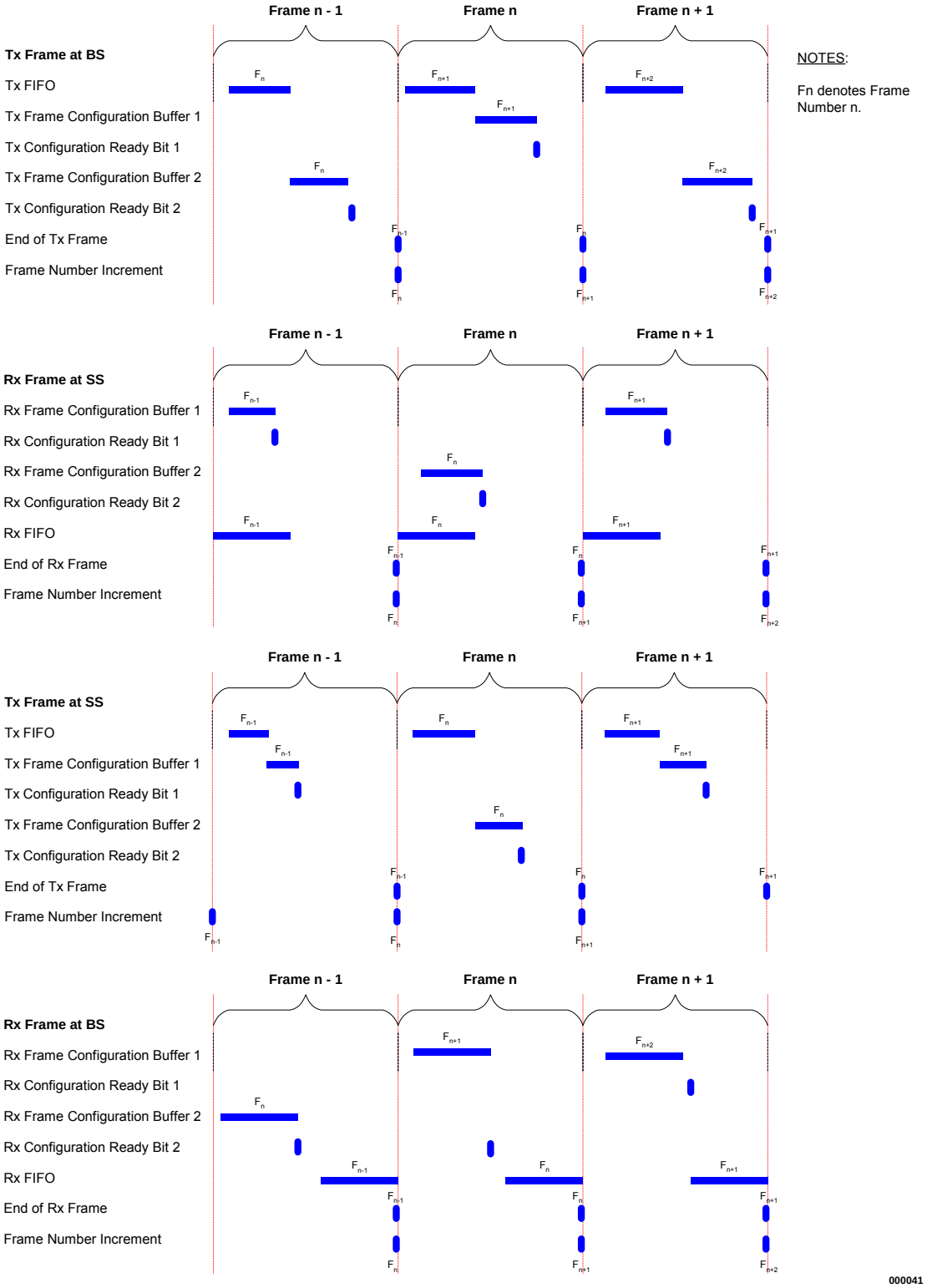


Figure 9: Frame Timing

3.5.1 Base Station Transmission Timing

Referring to Figure 8: TDD Framing, consider the following case where Tx Frame Descriptor 1 corresponds to ***DL Sub-Frame n – 1***. It has already been programmed and the corresponding data is being transmitted by the DM 256 (i.e.: in time, we are in ***DL Sub-Frame n – 1*** between ***A(n – 1***) and ***B(n – 1)***).

The MAC Layer must construct Tx Frame Descriptor 2 for Frame ***n***, transfer it to the DM 256 and the corresponding Ready bit must be set to 1 by the time the DM 256 expects to have a new Frame ready (refer also to Figure 9: Frame Timing) – in this case, the critical time is ***A(n)***: the beginning of the next ***DL Sub-Frame (Frame n)***. Note also that the transfer of the corresponding data to the Tx FIFO for each Tx Frame Descriptor should be initiated before the frame in which the data is required.

Frame n + 1 should now use Tx Frame Descriptor 1 but it may still be in use by the DM 256 as it is transmitting ***Frame n – 1***. In this case, the MAC Layer must delay until the Ready bit is reset to 0 by the DM 256. The MAC Layer can be informed of this event through the Tx EOF Interrupt that is triggered by the DM 256 at the end of the Frame at point ***C(n – 1)*** or the Ready bit can be polled until it has been cleared. The process continues for all subsequent Frames, toggling from Tx Frame Descriptor 1 and Tx Frame Descriptor 2, using the Tx EOF to signal that there is a new Tx Frame Descriptor free. Refer to Figure 9: Frame Timing

3.5.2 Subscriber Station Transmission Timing

Subscriber Station transmission timing differs from the Base Station since the Uplink stream is driven by the reception of an UL-MAP. Referring to Figure 8: TDD Framing consider the situation where a UL-MAP is received at point ***D(n – 1).***

At worst case, this gives the MAC Layer until ***B(n –1)***, the beginning of the UL Sub-Frame, to process the UL-MAP, decide the UL Allocation among the local CIDs (again, implementation specific), transfer the data to the Tx FIFO, build the Tx Frame Descriptor, transfer it to the DM 256 and set the 'Ready' bit. Refer to Figure 9: Frame Timing., an UL-MAP is generated in frame n-1, the corresponding frame configuration buffer is set fresh, and the UL-MAP is transmitted to all Subscribers in frame n-1. In this example, the content of this UL-MAP contains an allocation start time which refers to UL Bursts, allocated in frame n. Consequently, the frame number written into the Frame descriptor is that of n, and the UL-subframe applies to frame n. Clearly, for the Subscriber Station there is no danger of over-running the Tx Frame Descriptors since they are programmed and used within the scope of a single frame only one Tx Frame Descriptor is needed. However, the DM 256 is programmed to always toggle from one Tx Frame Descriptor to the other and therefore the MAC Layer must follow this convention as well.

3.5.3 Transfer of the Data Stream

Once the scheduling of the data to be transmitted has been decided, the stream needs to be transferred from MAC memory-space to the DM 256's Tx FIFO.

There are three methods that can be used:

- DMA,
- Serial or
- Memory-mapped writes.

3.5.3.1 Using DMA

Using DMA involves some processor or DMA Controller specific configuration (See Figure 39: DMA Reading and Write Timing Diagram). DMA offers several advantages and some disadvantages:

Table 13: Advantage and Disadvantage Of Using DMA

Advantages	Disadvantages
Offloads management of transfer from CPU: while the DMA Controller performs the data transfer, the CPU is free to perform other operations (such process received data).	Shared-bus: using DMA implies using the DM 256's parallel bus that is shared between the Tx and Rx FIFOs, the Tx and Rx Frame Descriptors as well as all register accesses.
Allows the DM 256 to control the transfer of the stream: by de-asserting the DMA-REQ line, the DM 256 can pause the transfer of a stream if the Tx FIFO is full and restart the transfer when some space is freed. In effect, this means that the MAC Layer can initiate a device-paced DMA transfer of the data to the Tx FIFO, then write the Tx Frame Descriptor and set the 'Ready' bit. When the DM 256 detects the beginning of the corresponding DL Sub-Frame, it will read the descriptor and empty the Tx FIFO as it processes the data for transmission. As the Tx FIFO is emptied, the DMA transfer will be re-enabled by the DM 256 until the transaction is complete.	Using DMA for transmission from the DM 256's perspective is very simple: set the Tx DMA bit to 1 in DMA Register 1 and the DM 256 will assert the DMA-REQ line when the Tx FIFO has space for another transfer and de-assert DMA-REQ when the Tx FIFO is full. Note that the DM 256 can auto-detect the bus width of the transfer through the assertion of the Write-Byte-Enable Lines. Therefore, there is no need to program the bus width on the DM 256 for transmission. A word of caution however when using DMA with a bus width other than byte wide: the DM 256 makes no association between the number of bytes specified by the Tx Frame Descriptor and the bus width used. That is, the DM 256 expects the correct number of bytes corresponding to the Tx Frame Descriptor regardless of the bus width used. Thus, if a 32-bit bus width is used and the total number of bytes for the Tx burst is say, 21 bytes, there would be 5 transfers of 4 bytes for 20 bytes and a final transfer must be of 1 byte only.
Multi-byte parallel bus width: the DM 256 uses the parallel interface which can accommodate 8 bit, 16 bit and 32 bit bus widths.	

To configuring the DM 256 for use with the by enabling the Tx and Rx Enable bits in the DMA Register.

3.5.3.2 Using the Serial Interface

The serial interface is intended for hardware-based MAC Layers and offers the same DM 256 controlled transfer advantage as DMA (See Figure 39: DMA Reading and Write Timing Diagram). That is, the DM 256 will de-assert the serial_in_ready_n line if the Tx FIFO is full. A further advantage is that the serial input line is a dedicated bus and does not suffer from delays caused by multiplexed bus contention.

Table 14: Advantage and Disadvantage Of Using Serial Interface

Advantages	Disadvantages
Allows the DM 256 to control the transfer of the stream: by de-asserting the serial_in_ready_n line, the DM 256 can pause the transfer of a stream if the Tx FIFO is full and restart the transfer when some space is freed. In effect, this means that the MAC Layer can initiate a transfer of the data to the Tx FIFO until it is full, then write the Tx Frame Descriptor and set the 'Ready' bit. When the DM 256 detects the beginning of the corresponding Tx Sub-Frame, it will read the descriptor and empty the Tx FIFO as it processes the data for transmission. As the Tx FIFO is emptied, the transfer will be re-enabled by the DM 256 until the transaction is complete.	Reduced maximum bandwidth: obviously, a serial interface offers lower maximum bandwidth than a parallel interface at 50 MHz but still meets the requirements of the most demanding PHY data rates.
Dedicated bus: the serial interface offers a dedicated bus to the Tx FIFO and does not share the bandwidth with other registers.	Designed for Hardware Interface: although it is possible to use the serial interface with a software based MAC, the implementation is more complex and would require polling of the serial_in_ready_n line to detect a full Tx FIFO.

To configuring the DM 256 for use with the Serial Interface by setting the Serial Port and Serial Mode bits in the Control Register to 1.

3.5.3.3 Using Memory-Mapped Writes

Using memory-mapped writes to the Tx FIFO is the last method available for transferring the data stream from MAC memory-space. This method is the least efficient however, since the Tx FIFO's byte count must be polled to avoid overflowing it and must be fast enough to avoid underflowing it.

Table 15: Advantage and Disadvantage of Memory-Mapped Writes

Advantages	Disadvantages
Multi-byte parallel bus width: the DM 256 uses the parallel interface which can accommodate 8 bit, 16 bit and 32 bit bus widths.	Polling: checking if the Tx FIFO is full is inefficient.

3.5.4 Construction of a Tx Frame Descriptor (Base Station)

Downlink bursts are specified by allocations in the DLFP and/or a DL MAP. The Tx Frame Descriptor used at the Base Station defines the frame structure of these DL Bursts. It also contains the DL Frame Prefix contained within the FCH burst.

3.5.4.1 Tx Frame Configuration at the Base Station

The Tx Frame Descriptor at the Base Station describes how to construct and when to transmit the DL sub-frame. The following subsections explain how to specify the symbols in the Tx Frame Descriptor.

Programming Notes	In general, a Slot Descriptor's Duration Field must be greater than or equal to the corresponding Symbol Descriptor's Length Field.

3.5.4.1.1 Frame Descriptor Section

Contained n the Frame Descriptor Section is the 802.16_Burst_Profile_to_Rate_ID and the 802.16_to_Wavesat_Rate_ID fields. This must always be filled with the byte value 0x00. These fields are only used in the Rx Frame Descriptor at the Subscriber Station. See Figure 10: Frame Descriptor for Tx Frame Configuration at Base Station and Subscriber Station, Rx Frame Configuration at the Base Station.

3.5.4.1.1.1 OFDM Frame Number: Specifying When to Transmit

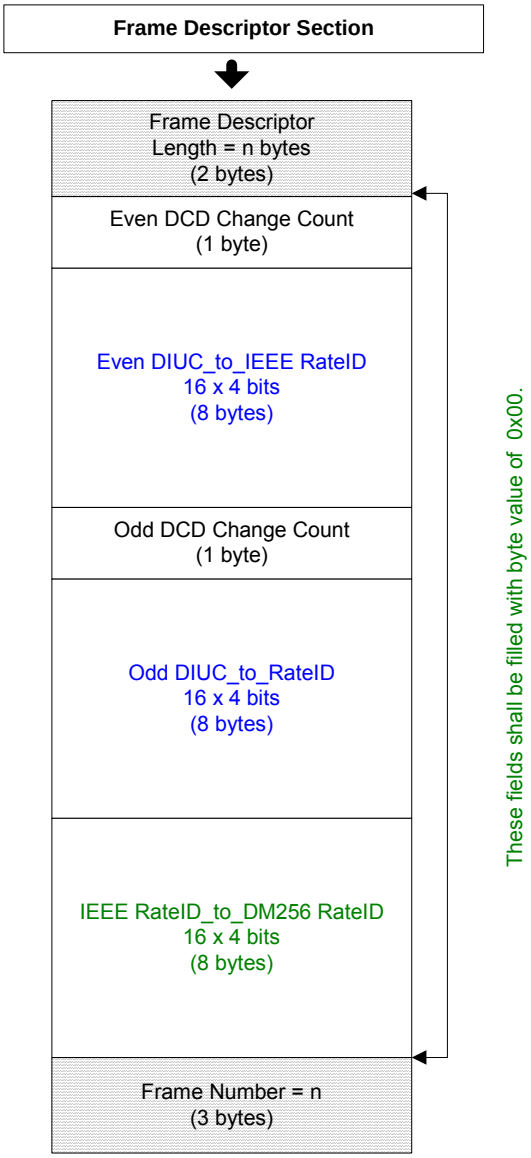
The OFDM Frame Number specifies the Frame in which the Tx Frame Descriptor applies. Since the Base Station acts as a reference, this value should start from zero at system startup and should be incremented by the MAC Layer for every subsequent Frame.

3.5.4.1.2 Burst Configuration and Burst Scheduling

3.5.4.1.2.1 DL Frame Prefix (DLFP)

The DLFP appears in the Burst Configuration Section and is used by the Subscriber Station to decode the first four DL-bursts. Refer to IEEE802.16-REVd/D5 for its precise format.

Programming Notes	The space available for the DLFP in the Burst Configuration Section is greater than the required space defined by IEEE802.16-2004. The unused space in the Burst Configuration Section's DLFP field must be padded with zeros.
	IEEE802.16-2004 defines a Header Checksum (HCS) field in the DLFP. The HCS is automatically calculated and inserted into the stream by the DM 256. Hence, it need not be accounted for when placing the DLFP data in the Burst Configuration Section.
	For every burst that the DLFP describes, a corresponding Symbol Descriptor and Slot Descriptor must be defined in the Tx Frame Descriptor.



Note: This Frame Descriptor is a Wavesat Proprietary Format.

000035.1

Figure 10: Frame Descriptor for Tx Frame Configuration at Base Station and Subscriber Station, Rx Frame Configuration at the Base Station.

3.5.4.1.2.2 Long Preamble

The DL sub-frame begins with the long preamble (REF1 followed by REF2). Therefore, the first two Symbol Descriptor elements in the Burst Configuration Section of the Tx Frame Descriptor should be a REF1 Symbol Descriptor followed by a REF2 Symbol Descriptor.

3.5.4.1.2.3 FCH Burst

The FCH (Frame Control Header) burst is one symbol long and follows the long preamble. Therefore, the FCH symbol type must be specified next after the long preamble in the Burst Configuration Section. Recall that the FCH contains the DLFP. Hence, during frame transmission, when DM 256 detects the FCH symbol type in the Frame Descriptor, it will insert the DLFP Data from the Frame Descriptor (generate and append HCS) into the stream from the Burst Configuration Section.

3.5.4.1.2.4 Short Preamble

The 802.16 standard provides for the option of a preamble to precede a DL burst. This is accomplished in the DM 256 by defining a symbol descriptor of length 1, and symbol type, REF2, immediately preceding the symbol descriptor describing the DL burst.

3.5.4.1.2.5 DL Bursts

The DL Bursts (1 to n bursts) immediately follow the FCH burst. A Symbol and Slot Descriptor must be defined for each DL Burst. DL Bursts may also be preceded by the short Preamble (REF2). See the Section 3.5.4.1.2.4. For every DL Burst, the DM 256 reads the corresponding amount of data from the Tx payload buffer. The DM 256 encodes and modulates the data using the parameters specified by the Symbol Descriptor and inserts the generated Data symbol(s) into the DL stream. If there is not enough data in the Tx Payload buffer to build the desired symbol, the DM 256 will leave the remaining data in the Tx Payload buffer and build the symbol using stuffing bytes of value 0xFF. Note that the Rate ID that is specified in the Symbol Descriptor for DL Bursts is not the IEEE802.16-2004 Rate ID but a Wavesat defined Rate ID. A conversion table is used to convert from IEEE Rate ID to Wavesat Rate ID, as defined in Table 16: 802.16-to-Wavesat Rate ID.

3.5.4.1.2.6 Gaps

A gap, during which no data is transmitted, may be inserted in the DL sub-frame. There are two methods to specify a Gap in the Tx Frame Descriptor at the Base Station:

- **Method A**: Offset the slot start time of the next Slot Descriptor where a gap is to be inserted. For example, if a Slot Descriptor ends at a count of 2720 samples and the next Slot Descriptor starts at a count of 3264 samples, then a gap of 544 samples is created.
- **Method B**: Specifying a slot duration that is greater than the slot duration actually required by the number of symbols specified in the corresponding Slot Descriptor. For example, if the Slot Descriptor specifies 10 symbols of 272 samples and the corresponding slot duration is 3264 samples, then the extra 544 samples have been used to create a gap.

3.5.5 Construction of a Tx Frame Descriptor (Subscriber Station)

Uplink bursts are specified by allocations provided in the form of an UL MAP, which is transmitted by the Base Station. These allocations specify the starting offset and duration of the burst. A UIUC code in the UL-MAP IE defines the type of the Uplink burst. A UCD (MAC Management Message) defines the burst profiles for Uplink access for a particular UIUC.

3.5.5.1 Tx Frame Configuration at the Subscriber Station

At the Subscriber Station, the Tx Frame Descriptor describes how to construct and when to transmit a UL Burst in the UL sub-frame. The following subsections explain how to specify the symbols in the Tx Frame Descriptor.

3.5.5.2 Frame Descriptor Section

See Figure 10: Frame Descriptor for Tx Frame Configuration at Base Station and Subscriber Station, Rx Frame Configuration at the Base Station.

3.5.5.2.1 OFDM Frame Number: Specifying When to Transmit

At the Subscriber Station, the OFDM Frame Number (specifying the Frame in which the Tx Frame Descriptor applies) is relative to the local DM 256's perception of the current Frame Number. The DM 256's 24-bit free-running Frame Count Register controls the perception of the current Frame Number. It is automatically initialized to 0 and is incremented every time the long preamble is detected (the beginning of a new DL subframe). Hence, the Frame Number at the Subscriber Station is not synchronized with that of the Base Station.

Consequently, an UL-MAP that describes the UL subframe for the current frame (ie: the Allocation Start Time is less than T_f (frame time)), then the OFDM Frame Number for the corresponding Tx Frame Descriptor should be the value in the Frame Count Register. Otherwise, the UL-MAP is describing the next frame, and the OFDM Frame Number for the corresponding Tx Frame Descriptor should be the value in the Frame Count Register plus one modulo 2^{24}.

3.5.5.2.2 DLFP, FCH and Conversion Tables

The DLFP and the FCH burst are not used in an UL subframe. However, since the DLFP is part of the Burst Configuration Section, all fields must be initialized with the byte value 0x00. Once again, the tables containing 802.16 Burst Profile to Rate ID and the table 802.16 to Wavesat Rate ID in the Frame Descriptor Section, is initialized with the byte value 0x00.

3.5.5.3 Burst Configuration and Burst Scheduling

Programming Notes	The Duration field in the Slot Descriptor corresponds to the Length in the Symbol Descriptor.

3.5.5.3.1 Initial Ranging Interval / Bandwidth Request Interval

The Initial Ranging Interval and the Bandwidth Request Interval are each made up of a number of transmission opportunities as defined by the UL-MAP and UCD Message.

Each of these symbols must be specified for each transmission opportunity. Both intervals may contain multiple transmission opportunities. The method of choosing a transmission opportunity is made by the MAC Layer and is clearly defined by IEEE802.16-2004. Once a transmission opportunity is chosen, the Slot Start Time must be programmed accordingly.

3.5.5.3.2 Midambles and Postambles

Midambles may be inserted every ***n*** Data Symbols as specified by the UL-MAP. In the Tx Frame Descriptor at the Subscriber Station, each of these symbols must be specified.

3.5.5.3.3 UL Bursts

A UL burst can be made up of the following symbols:

• REF2 symbol (short preamble).
• Data symbols.

The UL bursts are defined by filling out the symbol descriptor fields accordingly. Once again, the Rate ID used in the symbol descriptor field is the Wavesat Rate ID. A conversion table is used to convert from IEEE Rate ID to Wavesat Rate ID, as defined in Table 16: 802.16-to-Wavesat Rate ID. Note that IEEE802.16-2004 clearly specifies which UIUC codes require the use of the Long or Short Preambles and the Subscriber's Tx Frame Descriptor must be constructed accordingly.

With this information, UL bursts may be programmed for a given frame. This is accomplished by translating the start time in the UL-MAP IE, to a corresponding offset within a given frame, measured in samples. Similar to the Base Station, one or more Burst and Schedule descriptor pairs are created for the type of Uplink access specified by the UL-MAP IE.

3.6 Data Reception from the DM 256

Much like Data Transmission, a pair of Rx Frame Descriptors drives reception with the DM 256. The DM 256 will toggle from using one Rx Frame Descriptor to the other. These Rx Descriptors indicate how the DM 256 should demodulate/decode the incoming stream of data.

Unlike Data Transmission however, the stream of data extracted from the Rx FIFO is not simply the raw data transmitted by the other endpoint. That is to say that at the Transmission end, the MAC Layer sends MAC PDUs (MAC Headers, accompanying payload and CRC if applicable) to the DM 256 while at the Receiving end, the DM 256 does not send MAC PDUs alone to the MAC Layer. The DM 256 prepends every symbol with a Statistical Header that includes a length field that indicates how many bytes in the uncoded block follow (since the uncoded block size is a function of the modulation/coding used). This implies that the receiving MAC Layer immediately above the DM 256 must re-assemble the MAC PDUs from the fragments of uncoded data blocks separated by the statistical header.

Note that a MAC PDU will likely span over several OFDM Symbols and thus, a single MAC PDU may have several statistical headers that apply and that an OFDM Symbol does not necessarily start with a MAC Header except at the beginning of a burst:

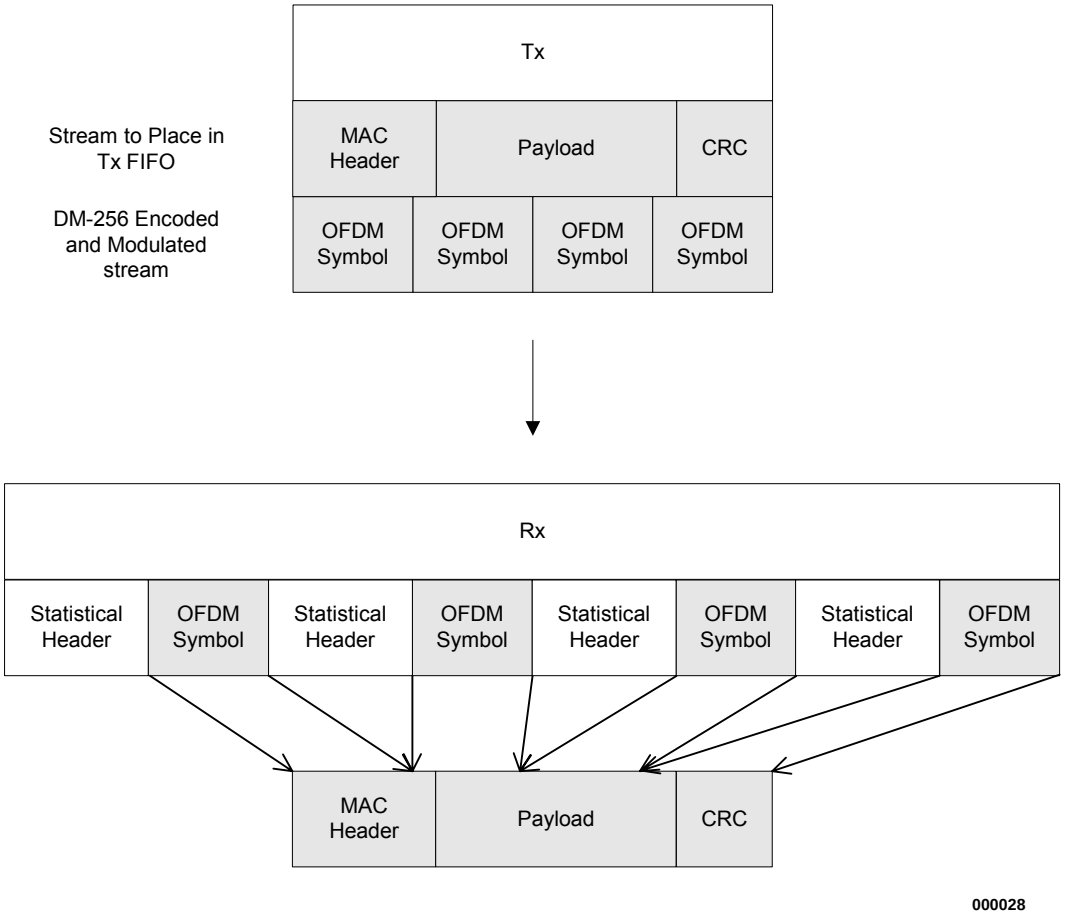


Figure 11: Data Reception of DM 256

The question arises of how to interpret the statistics when several sets may apply to a single MAC PDU. The answer is in fact MAC Layer implementation specific as well as Base Station and Subscriber Station specific.

3.6.1 Base Station Reception Timing

Reception at the Base Station is in reality, the reception of the UL Sub-Frame. Recall that the UL Sub-Frame is in fact defined by the Base Station and corresponds to the UL-MAP. Hence, once the MAC Layer creates the UL-MAP, the corresponding Rx Frame Descriptor should also be created, written to the DM 256 and the 'Ready' bit set before the beginning of the corresponding UL Sub-Frame (point B). Refer to Figure 9: Frame Timing.

3.6.1.1 Transferring the Stream

Because the Base Station does not know whether a Subscriber will actually transmit a burst in the UL sub-frame, the MAC Layer can not make any assumptions about the expected quantity of data. As such, the only feasible option is to transfer a Statistical header followed by the corresponding uncoded data block (whose length is given in the Statistical header), each being processed as it arrives ensuring low latency.

Note that this strategy is better suited to the DMA and Serial Interfaces because of their ability to halt a transfer when the Rx FIFO is empty and to use interrupts to notify the completion of another transfer. In effect, the DMA or Serial Controller can be programmed to first transfer a Statistical header. Once the transfer is complete, the length of the following uncoded data block is extracted from the Statistical header and the DMA or Serial Controller can be programmed to perform the transfer of that uncoded data block.

With Memory-mapped reads, if the Rx FIFO is empty, MAC Layer must rely on the Rx EOF Frame interrupt. This interrupt (when enabled) triggers on the reception of a Short Preamble (REF2) and can thus serve to indicate that there is data available in the Rx FIFO to be read. Of course, if the data is read faster than the DM 256 can fill the Rx FIFO, the Rx FIFO count must be polled to ensure that the MAC Layer is not reading from an empty FIFO.

3.6.2 Subscriber Station Reception Timing

Reception at the Subscriber Station is in reality the reception of the DL Sub-Frame. Recall that the DLFP and the DL-MAP define the DL Sub-Frame. The DM 256 automatically decodes the DLFP and hence, the first four bursts are demodulated and decoded without any MAC intervention on a frame-by-frame basis. However, if the DL Sub-Frame contains more than four bursts or any Extended Information Elements, the Base Station will send a DL-MAP that must be decoded by the MAC Layer. Referring to Figure 8: TDD Framing, consider Frame n, where D(n) is the point in the DL Sub-Frame when the DL-MAP is received and E(n) the first instance that the DL-MAP describes. The MAC Layer has between D(n) and E(n) to retrieve the DL-MAP from the Rx FIFO, decode the Information Elements contained within, construct a corresponding Rx Frame Descriptor, write it to the DM 256 and set the 'Ready' bit. This is also depicted in Refer to Figure 9: Frame Timing.

3.6.2.1 Transferring the Stream

The Subscriber Station MAC Layer has no way of knowing what to expect in the downstream direction. Thus, the only option is to transfer Statistical headers and Uncoded data blocks as they are received by the DM 256 continuously. Clearly the DMA and Serial Interface are optimal in this situation for the same reasons as for Transmission: if the Rx FIFO is empty, the DM 256 halts the transfer and both interfaces should be able to signal the completion via an interrupt. The operation is to simply program the DMA or Serial Interface to transfer a Statistical header. Upon completion, the length of the Uncoded data block is extracted from the Statistical header and the DMA or Serial Interface is programmed for the transfer of the Uncoded data block. Then the transfer for the next Statistical header is programmed immediately. If the Rx FIFO is empty, then the transfer will pause until the Statistical header is received by the DM 256 and the process repeats.

With Memory-mapped reads, if the Rx FIFO is empty, MAC Layer must rely on the Rx EOF Frame interrupt. This interrupt (when enabled) triggers on the reception of a Short Preamble (REF2) and can thus serve to indicate that there is data available in the Rx FIFO to be read. Of course, if the data is read faster

than the DM 256 can fill the Rx FIFO, the Rx FIFO count must be polled to ensure that the MAC Layer is not reading from an empty FIFO.

3.6.3 Construction of a Rx Frame Descriptor (Base Station)

The Rx Frame Descriptor describes the content of a single frame, containing zero or more UL allocations defined by the UL-MAP.

3.6.3.1 Frame Descriptor Section

The DLFP and the FCH burst are not used in an UL subframe. However, since the DLFP is part of the Burst Configuration Section, all fields must be initialized with the byte value 0x00. Once again, the tables containing 802.16 Burst Profile to Rate ID and the table 802.16 to Wavesat Rate ID in the Frame Descriptor Section, is initialized with the byte value 0x00. The Frame Number described in the Frame Description section is the current frame number being used during transmission. See Figure 10: Frame Descriptor for Tx Frame Configuration at Base Station and Subscriber Station, Rx Frame Configuration at the Base Station.

3.6.3.2 Burst Configuration and Burst Scheduling

3.6.3.2.1 Initial Ranging Interval / Bandwidth Request Interval

The Initial Ranging Interval and the Bandwidth Request Interval are each made up of a number of transmission opportunities as defined by the UL-MAP and UCD Messages. A Symbol Descriptor and Schedule Descriptor pair must be defined for each Transmission Opportunity.

The Length field in the Symbol Descriptor must specify only the number of data symbols contained in the burst while the Slot Duration in the Schedule Descriptor must account for all symbols (REF1, REF2 and Data).

3.6.3.2.2 UL Bursts

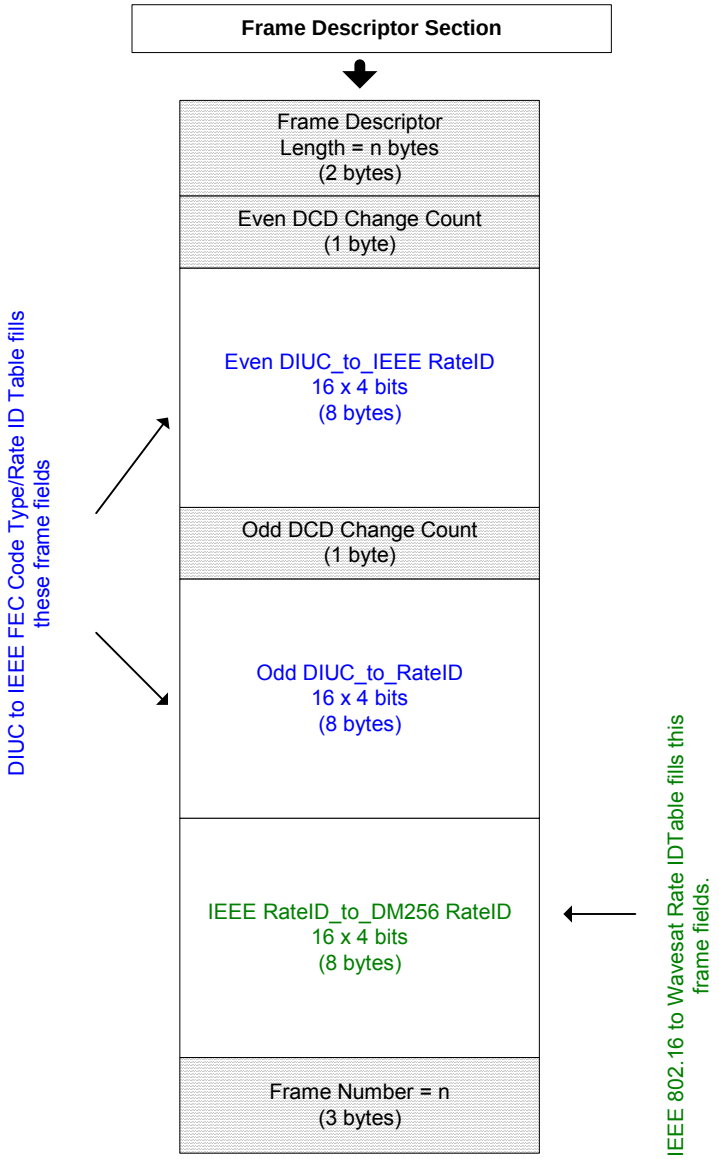
At the Base Station, the long preambles and midambles received in the UL are automatically detected. The Length field in the Symbol Descriptor must specify only the number of Data symbols contained in the burst while the Slot Duration in the Slot Descriptor must account for all symbols (REF2 symbol, Midamble symbols and Data symbols) contained in the burst. The Slot Duration field of a Slot Descriptor is set to the length of the allocation specified in the Duration field of the UL-MAP IE.

3.6.4 Construction of a Rx Frame Descriptor (Subscriber Station)

The Rx Frame Descriptor at the Subscriber Station describes how to receive and deconstruct the DL sub-frame.

3.6.4.1 Frame Descriptor Section

The first four allocations are described by the content of the DLFP, which is transmitted in the FCH burst and decoded by the DM 256. In order to decode the content of the DLFP, the 802.16 Burst Profile to Rate ID tables and the 802.16 to Wavesat Rate ID tables must be loaded into the Frame Description section of the Rx Frame Descriptor and the Rx Frame Descriptor status/control register must be set to 1. See Figure 12: Frame Descriptor Section Details on DIUC to IEEE FEC Code Type/Rate ID and IEEE 802.16 to Wavesat Rate ID.



Note: This Frame Descriptor is a Wavesat Proprietary Format.

000035

Figure 12: Frame Descriptor Section Details on DIUC to IEEE FEC Code Type/Rate ID and IEEE 802.16 to Wavesat Rate ID

3.6.4.2 Burst Configuration and Burst Schedule

3.6.4.2.1 Long Preamble

The long preamble is not specified in the Rx Frame Descriptor. When a frame is received at a Subscriber Station, the long preamble is automatically detected.

3.6.4.2.2 FCH burst

The FCH burst is not specified in the Frame Descriptor. When the FCH burst is received, it is automatically decoded using the mandatory BPSK-1/2 modulation scheme (Wavesat Rate ID = 6) to extract the DL Frame Prefix.

3.6.4.2.3 DL bursts 1-4

DL bursts 1-4 are not specified in the Frame Descriptor as they are decoded by the DM 256 via the DL Frame Prefix (DLFP) in the FCH burst. The Rx Frame Descriptor at the Subscriber Station can be created only after the DL-MAP Message is received and processed. The MAC Layer must then use the DL-MAP to write the Rx Frame Descriptor, which describes the remaining bursts inside the DL sub-frame.

3.6.4.2.4 DL burst 5…n

All remaining bursts in the DL sub-frame must be defined in the Frame Descriptor using their respective burst profiles specified in the DL-MAP. Each DL burst is made up of Data symbols, which specify when to expect payload and how it must be decoded. If a preamble is specified in the DL-MAP for any of the DL bursts, the Slot Duration field in the Slot Descriptor must account for all symbols (REF2 symbol and Data symbols) contained in the burst. The Symbol Count in the Symbol Descriptor must account only for the Data Symbols.

3.6.4.2.5 Gaps

When a Gap interval is specified in the DL-MAP, a corresponding Symbol and Slot Descriptor pair must be defined in the Rx Frame Descriptor. The Length field in the Symbol Descriptor and the Slot Duration field in the Slot Descriptor correspond to the Duration specified by the Gap Interval in the DL-MAP. Note that the DM 256 will demodulate the number of symbols using the Wavesat Rate ID specified in the Symbol Descriptor and will place a Statistical header and one uncoded data block of undefined data for each Gap symbol in the interval.

Some of the Wavesat Rate IDs indicates how the DM 256 should process the symbol. A Wavesat Rate ID of 14 is used to indicate that the corresponding IEEE Rate ID is unsupported. The DM 256 will make no attempt to demodulate symbols with this type. It will, however, keep track of the length of the allocation and skip over it. A Wavesat Rate ID of 15 is used to indicate that the Rate ID is unknown and nothing should be done. A Wavesat Rate ID of 13 is used to indicate a GAP in transmission. The DM 256 will insert a GAP symbol type into the Rx Configuration Processor so that the DM 256 will take measurements during this period.

The remainder of the DLFP is used to specify DL allocations using DIUC codes. Since the DIUC codes reference burst profiles described in the DCD message, these tables must be loaded initially with values that map to unsupported Wavesat Rate Ids. DL allocations specified by DIUC cannot be decoded until a valid DCD message is received. When a DCD message is received, another Rx Frame Descriptor is created describing the change to the tables and activated in the DM 256 for the subsequent frame. Since it is not deterministic when a DCD message with an incremented change count is received (this is known only from the DCD change count field in the DLFP or in the DL-MAP), two 802.16 Burst Profile to Rate ID tables are provided with associated change counts fields. These tables are labeled as even and odd, such that when a new DCD message is received having a odd change count, it goes into the odd table, and a DCD having a even change count goes into a even table. When a DLFP is received it is compared with the value contained in the two tables. If there is a match, then the profiles referenced by DIUC code are then decoded. The DIUC contained in the DLFP is used as an index to the 802.16 Burst Profile to Rate ID table. The value contained in this table is then used as an index into the 802.16 to Wavesat Rate ID table. This indicates to the DM 256, which FEC code to use to demodulate the DL allocation or which action it should take. The IEEE 802.16 standard predefines several DIUC codes. For example, STC Zone (DIUC=0), reserved (DIUC=12), GAP (DIUC=13), End-of-MAP (DIUC=14), and Extended DIUC (DIUC=15). Of these, special codes, DIUC 12, 14, and 15 should never appear in the DLFP. DIUC=13 may appear and is mapped to Wavesat Rate ID 13. Appearance of DIUC=13 causes the DM 256 to automatically insert a GAP symbol for the duration specified.

The format of the Frame Descriptor Section is shown below in Figure 12: Frame Descriptor Section Details on DIUC to IEEE FEC Code Type/Rate ID and IEEE 802.16 to Wavesat Rate ID. This figure illustrates how Table 16: 802.16-to-Wavesat Rate ID and Table 17: DIUC vs IEEE FEC Code Type/Rate ID are contained within the Frame Descriptor Section.

3.7 Scheduling Notes

3.7.1 Viterbi Tail Byte

The Viterbi tail byte is a byte of value 0x00 which is inserted by the DM 256 at the end of each burst and must be taken into account when scheduling. The implication is that when scheduling, the last byte of the last data block in every burst must be reserved for the Viterbi tail byte. A burst (DL or UL) is considered to be a set of ***n*** symbols using the same modulation and coding rate.

3.7.2 Padding

To avoid transmission underruns, a burst must be padded to the allocation defined by the DL-MAP IE or UL-MAP IE, less the reserved byte for the Viterbi tail byte.

3.7.3 A Scheduling Example

For example:

Assume that a DL-MAP IE defines a burst allocation = 5 symbols (using a modulation/coding rate of QPSK-1/2).

Total available allocation = ((5 * 24 bytes/uncoded data block) – 1 byte for the Viterbi tail byte).

Allocation is 119 bytes.

Refer to Figure 13: Mapping MAC PDUs to DL Bursts.

MAC PDU #1 = 57 bytes

MAC PDU #2 = 47 bytes.

Total allocations = 57 bytes + 47 bytes = 104 bytes.

The DM 256 would have an underrun, unless an addition of 119 bytes – 104 bytes = 15 bytes of padding data is transferred into the Tx FIFO.

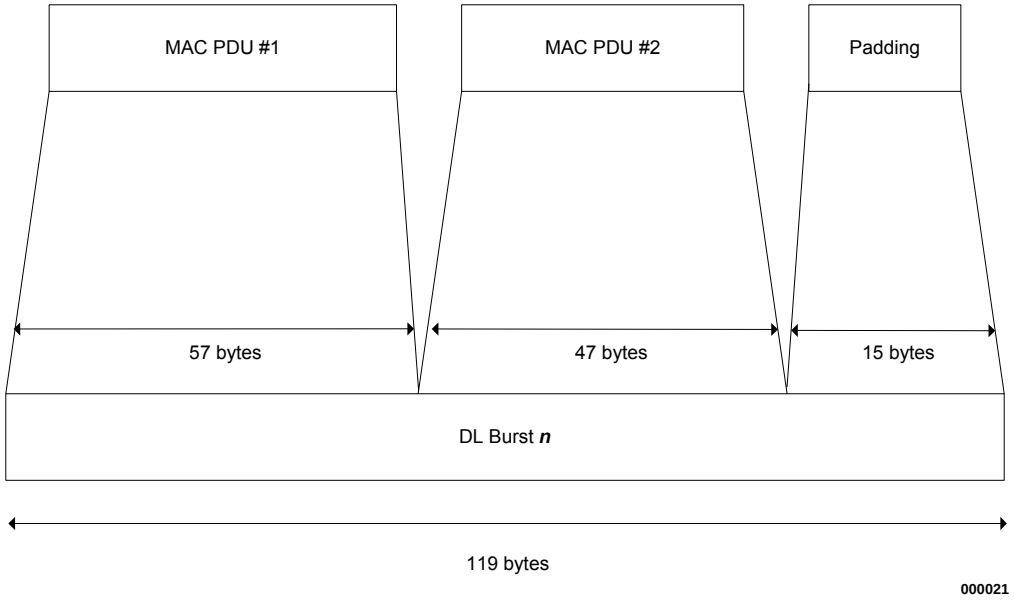


Figure 13: Mapping MAC PDUs to DL Bursts

3.7.4 Base Station Scheduling Notes

3.7.4.1 TTG/RTG

In TDD framing, the IEEE 802.16 standard specifies a value for TTG and RTG to be inserted between the DL subframe and UL subframe. The frame duration is specified in the Burst Configuration Section with the field labeled Frame Size. In order to insert a gap for TTG, the first UL-MAP IE will have its Start Time field indicated by the length of the DL subframe plus the TTG value. The start time is specified in samples. Note that IEEE802.16-2004 mandates the TTG be specified in Physical Slots (PS). However, the value for TTG must also be expressed in samples for the DM 256.

For the desired value of RTG, the total allocation for the UL subframe must not exceed the sum of the DL subframe plus the value of TTG and RTG (expressed in samples).

3.8 Using the Conversion Tables

IEEE802.16-2004 mandates that the DLFP (for DL bursts 2 to 4) and a DL-MAP IE, defines the interval type or the burst profile to be used, through DIUC code. DIUC codes 1 to 11 are mapped to a IEEE FEC Code Type/Rate ID. The DCD Message defines that mapping.

However, the DM 256 does not use the same Rate ID numbering as the official standard. As a result, a two-level conversion must be performed: first from DIUC to IEEE FEC Code Type/Rate ID and then from IEEE FEC Code Type/Rate ID to DM 256 Rate ID.

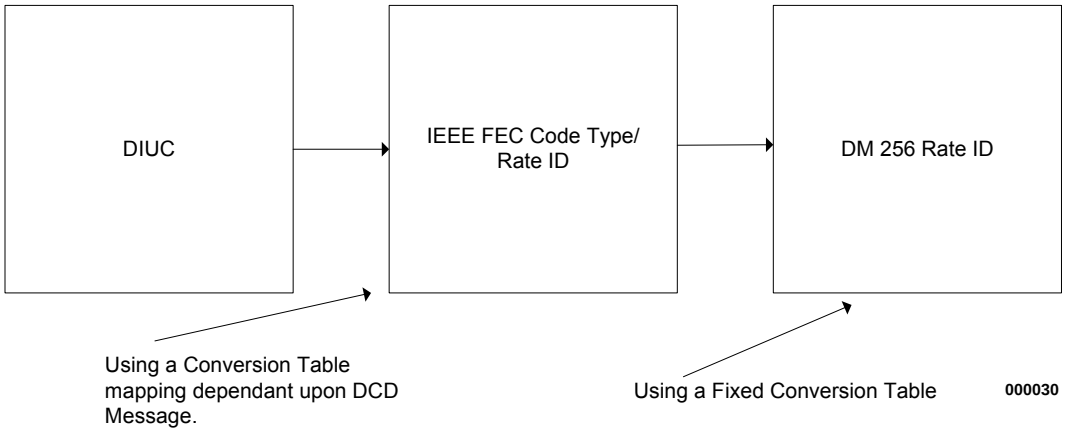


Figure 14: How and Where Conversion Tables are Used

The Table 16: 802.16-to-Wavesat Rate ID defines the mapping from IEEE FEC Code Type/Rate ID to DM 256 Rate ID. This mapping is fixed and does not change.

Table 16: 802.16-to-Wavesat Rate ID

IEEE FEC Code Type/ Rate ID	*DM 256 Rate ID*
0 BPSK-1/2	6
1 QPSK-1/2	0
2 QPSK-3/4	1
3 QAM16-1/2	2
4 QAM16-3/4	3
5 QAM64-2/3	4
6 QAM64-3/4	5
7 Reserved	14
8 Reserved	14
9 Reserved	14
10 Reserved	14
11 Reserved	14
12 Reserved	14
13 Reserved	13
14 Reserved	15
15 Reserved	15

Note:

DM 256 only supports IEEE FEC Code Type/Rate ID 0 to 6.

DM 256 Rate ID 7 to 12 are Reserved and should not be used.

DM 256 Rate ID 13 indicates that the DM 256 should insert a Gap Symbol whose length is defined by the DLFP-IE.

DM 256 Rate ID 14 instructs the DM 256 to count the number of symbols indicated by the length in the DLFP-IE time but not decode them.

DM 256 Rate ID 15 instructs the DM 256 to do nothing for the number of symbols indicated by the length in the DLFP-IE.

This implies that for DIUC Codes that map to a supported IEEE FEC Code Type/Rate ID, and the IEEE FEC Code Type/Rate ID can be used to directly index the DM 256 Rate ID.

Consider the following mapping example of DIUC to IEEE FEC Code Type/Rate ID:

DUIC 5 maps to IEEE Rate 3, then we see immediately from the Table, that the appropriate DM 256 Rate ID to use is 2). On the other hand, DIUC Codes that map to an unsupported IEEE Rate ID should index IEEE Rate ID 7 and thus use DM 256 Rate ID 14. Also of note is DIUC Code 0, the STC Zone Code. This should be mapped to IEEE Rate ID 15 and thus use DM 256 Rate ID 15. Finally, DIUC Code 13, the Gap Code, should be mapped to IEEE Rate ID 13 and thus use DM 256 Rate ID 13.

Table 17: DIUC vs IEEE FEC Code Type/Rate ID

DIUC	*IEEE FEC Code Type/ Rate ID*
1	0 (BPSK-1/2)
2	3 (QAM16-1/2)
3	6 (QAM64-3/4)
4	2 (QPSK-3/4)
5	11 (QAM64-BTC-2/3)
6	9 (QAM16-BTC-3/5)
7	17 (QAM16-CTC-3/4)
8	19 (QAM64-CTC-3/4)
9	7 (QPSK-BTC-1/2)
10	4 (QPSK-3/4)
11	1 (QPSK-1/2)

The following DIUC to Rate-ID Table is written to the Frame Descriptor Section of the Rx Frame Descriptor.

Table 18: Example Rate ID Mappings

DIUC Code	Index to IEEE FEC Code Type/Rate ID to DM-256Rate ID Table
DIUC 0	15
DIUC 1	0
DIUC 2	3
DIUC 3	6
DIUC 4	2
DIUC 5	7
DIUC 6	7
DIUC 7	7
DIUC 8	7
DIUC 9	7
DIUC 10	4
DIUC 11	1
DIUC 12	7
DIUC 13	13
DIUC 14	15
DIUC 15	15

IEEE FEC Code Type/Rate ID	*DM-256 Rate ID*
0	6
1	0
2	1
3	2
4	3
5	4
6	5
7	14
8	14
9	14
10	14
11	14
12	14
13	13
14	15
15	15

000029

3.9 Frame Parameters

3.9.1 Frame Duration Code 0

Table 19: Frame Duration Code 0

Channel Bandwidth (MHz)	CP Size	Sampling Frequency (MHz)	Symbol Time (μs)	Frame Duration (ms)	Samples/ Frame	PS/Frame	Symbols/ Frame
	1/4	2.000	160.000	2.50	5000.00	1250.00	15.00
	1/8	2.000	144.000	2.50	5000.00	1250.00	17.00
	1/16	2.000	136.000	2.50	5000.00	1250.00	18.00
1.75	1/32	2.000	132.000	2.50	5000.00	1250.00	18.00
	1/4	4.000	80.000	2.50	10000.00	2500.00	31.00
	1/8	4.000	72.000	2.50	10000.00	2500.00	34.00
	1/16	4.000	68.000	2.50	10000.00	2500.00	36.00
3.5	1/32	4.000	66.000	2.50	10000.00	2500.00	37.00
	1/4	8.000	40.000	2.50	20000.00	5000.00	62.00
	1/8	8.000	36.000	2.50	20000.00	5000.00	69.00
	1/16	8.000	34.000	2.50	20000.00	5000.00	73.00
7	1/32	8.000	33.000	2.50	20000.00	5000.00	75.00
	1/4	11.520	27.778	2.50	28800.00	7200.00	90.00
	1/8	11.520	25.000	2.50	28800.00	7200.00	100.00
	1/16	11.520	23.611	2.50	28800.00	7200.00	105.00
10	1/32	11.520	22.917	2.50	28800.00	7200.00	109.00

3.9.2 Frame Duration Code 1

Table 20: Frame Duration Code 1

Channel Bandwidth (MHz)	CP Size	Sampling Frequency (MHz)	Symbol Time (μs)	Frame Duration (ms)	Samples/ Frame	PS/Frame	Symbols/ Frame
	1/4	2.000	160.000	4.00	8000.00	2000.00	25.00
	1/8	2.000	144.000	4.00	8000.00	2000.00	27.00
	1/16	2.000	136.000	4.00	8000.00	2000.00	29.00
1.75	1/32	2.000	132.000	4.00	8000.00	2000.00	30.00
	1/4	4.000	80.000	4.00	16000.00	4000.00	50.00
	1/8	4.000	72.000	4.00	16000.00	4000.00	55.00
	1/16	4.000	68.000	4.00	16000.00	4000.00	58.00
3.5	1/32	4.000	66.000	4.00	16000.00	4000.00	60.00
	1/4	8.000	40.000	4.00	32000.00	8000.00	100.00
	1/8	8.000	36.000	4.00	32000.00	8000.00	111.00
	1/16	8.000	34.000	4.00	32000.00	8000.00	117.00
7	1/32	8.000	33.000	4.00	32000.00	8000.00	121.00
	1/4	11.520	27.778	4.00	46080.00	11520.00	144.00
	1/8	11.520	25.000	4.00	46080.00	11520.00	160.00
	1/16	11.520	23.611	4.00	46080.00	11520.00	169.00
10	1/32	11.520	22.917	4.00	46080.00	11520.00	174.00

3.9.3 Frame Duration Code 2

Table 21: Frame Duration Code 2

Channel Bandwidth (MHz)	CP Size	Sampling Frequency (MHz)	Symbol Time (µs)	Frame Duration (ms)	Samples/ Frame	PS/Frame	Symbols/ Frame
	1/4	2.000	160.000	5.00	10000.00	2500.00	31.00
	1/8	2.000	144.000	5.00	10000.00	2500.00	34.00
	1/16	2.000	136.000	5.00	10000.00	2500.00	36.00
1.75	1/32	2.000	132.000	5.00	10000.00	2500.00	37.00
	1/4	4.000	80.000	5.00	20000.00	5000.00	62.00
	1/8	4.000	72.000	5.00	20000.00	5000.00	69.00
	1/16	4.000	68.000	5.00	20000.00	5000.00	73.00
3.5	1/32	4.000	66.000	5.00	20000.00	5000.00	75.00
	1/4	8.000	40.000	5.00	40000.00	10000.00	125.00
	1/8	8.000	36.000	5.00	40000.00	10000.00	138.00
	1/16	8.000	34.000	5.00	40000.00	10000.00	147.00
7	1/32	8.000	33.000	5.00	40000.00	10000.00	151.00
	1/4	11.520	27.778	5.00	57600.00	14400.00	180.00
	1/8	11.520	25.000	5.00	57600.00	14400.00	200.00
	1/16	11.520	23.611	5.00	57600.00	14400.00	211.00
10	1/32	11.520	22.917	5.00	57600.00	14400.00	218.00

3.9.4 Frame Duration Code 3

Table 22: Frame Duration Code 3

Channel Bandwidth (MHz)	CP Size	Sampling Frequency (MHz)	Symbol Time (µs)	Frame Duration (ms)	Samples/ Frame	PS/Frame	Symbols/ Frame
	1/4	2.000	160.000	8.00	16000.00	4000.00	50.00
	1/8	2.000	144.000	8.00	16000.00	4000.00	55.00
	1/16	2.000	136.000	8.00	16000.00	4000.00	58.00
1.75	1/32	2.000	132.000	8.00	16000.00	4000.00	60.00
	1/4	4.000	80.000	8.00	32000.00	8000.00	100.00
	1/8	4.000	72.000	8.00	32000.00	8000.00	111.00
	1/16	4.000	68.000	8.00	32000.00	8000.00	117.00
3.5	1/32	4.000	66.000	8.00	32000.00	8000.00	121.00
	1/4	8.000	40.000	8.00	64000.00	16000.00	200.00
	1/8	8.000	36.000	8.00	64000.00	16000.00	222.00
	1/16	8.000	34.000	8.00	64000.00	16000.00	235.00
7	1/32	8.000	33.000	8.00	64000.00	16000.00	242.00
	1/4	11.520	27.778	8.00	92160.00	23040.00	288.00
	1/8	11.520	25.000	8.00	92160.00	23040.00	320.00
	1/16	11.520	23.611	8.00	92160.00	23040.00	338.00
10	1/32	11.520	22.917	8.00	92160.00	23040.00	349.00

3.9.5 Frame Duration Code 4

Table 23: Frame Duration Code 4

Channel Bandwidth (MHz)	CP Size	Sampling Frequency (MHz)	Symbol Time (μs)	Frame Duration (ms)	Samples/ Frame	PS/Frame	Symbols/ Frame
	1/4	2.000	160.000	10.00	20000.00	5000.00	62.00
	1/8	2.000	144.000	10.00	20000.00	5000.00	69.00
	1/16	2.000	136.000	10.00	20000.00	5000.00	73.00
1.75	1/32	2.000	132.000	10.00	20000.00	5000.00	75.00
	1/4	4.000	80.000	10.00	40000.00	10000.00	125.00
	1/8	4.000	72.000	10.00	40000.00	10000.00	138.00
	1/16	4.000	68.000	10.00	40000.00	10000.00	147.00
3.5	1/32	4.000	66.000	10.00	40000.00	10000.00	151.00
	1/4	8.000	40.000	10.00	80000.00	20000.00	250.00
	1/8	8.000	36.000	10.00	80000.00	20000.00	277.00
	1/16	8.000	34.000	10.00	80000.00	20000.00	294.00
7	1/32	8.000	33.000	10.00	80000.00	20000.00	303.00
	1/4	11.520	27.778	10.00	115200.00	28800.00	360.00
	1/8	11.520	25.000	10.00	115200.00	28800.00	400.00
	1/16	11.520	23.611	10.00	115200.00	28800.00	423.00
10	1/32	11.520	22.917	10.00	115200.00	28800.00	436.00

3.9.6 Frame Duration Code 5

Table 24: Frame Duration Code 5

Channel Bandwidth (MHz)	CP Size	Sampling Frequency (MHz)	Symbol Time (μs)	Frame Duration (ms)	Samples/ Frame	PS/Frame	Symbols/ Frame
	1/4	2.000	160.000	12.50	25000.00	6250.00	78.00
	1/8	2.000	144.000	12.50	25000.00	6250.00	86.00
	1/16	2.000	136.000	12.50	25000.00	6250.00	91.00
1.75	1/32	2.000	132.000	12.50	25000.00	6250.00	94.00
	1/4	4.000	80.000	12.50	50000.00	12500.00	156.00
	1/8	4.000	72.000	12.50	50000.00	12500.00	173.00
	1/16	4.000	68.000	12.50	50000.00	12500.00	183.00
3.5	1/32	4.000	66.000	12.50	50000.00	12500.00	189.00
	1/4	8.000	40.000	12.50	100000.00	25000.00	312.00
	1/8	8.000	36.000	12.50	100000.00	25000.00	347.00
	1/16	8.000	34.000	12.50	100000.00	25000.00	367.00
7	1/32	8.000	33.000	12.50	100000.00	25000.00	378.00
	1/4	11.520	27.778	12.50	144000.00	36000.00	450.00
	1/8	11.520	25.000	12.50	144000.00	36000.00	500.00
	1/16	11.520	23.611	12.50	144000.00	36000.00	529.00
10	1/32	11.520	22.917	12.50	144000.00	36000.00	545.00

3.9.7 Frame Duration Code 6

Table 25: Frame Duration Code 6

Channel Bandwidth (MHz)	CP Size	Sampling Frequency (MHz)	Symbol Time (µs)	Frame Duration (ms)	Samples/ Frame	PS/Frame	Symbols/ Frame
	1/4	2.000	160.000	20.00	40000.00	10000.00	125.00
	1/8	2.000	144.000	20.00	40000.00	10000.00	138.00
	1/16	2.000	136.000	20.00	40000.00	10000.00	147.00
1.75	1/32	2.000	132.000	20.00	40000.00	10000.00	151.00
	1/4	4.000	80.000	20.00	80000.00	20000.00	250.00
	1/8	4.000	72.000	20.00	80000.00	20000.00	277.00
	1/16	4.000	68.000	20.00	80000.00	20000.00	294.00
3.5	1/32	4.000	66.000	20.00	80000.00	20000.00	303.00
	1/4	8.000	40.000	20.00	160000.00	40000.00	500.00
	1/8	8.000	36.000	20.00	160000.00	40000.00	555.00
	1/16	8.000	34.000	20.00	160000.00	40000.00	588.00
7	1/32	8.000	33.000	20.00	160000.00	40000.00	606.00
	1/4	11.520	27.778	20.00	230400.00	57600.00	720.00
	1/8	11.520	25.000	20.00	230400.00	57600.00	800.00
	1/16	11.520	23.611	20.00	230400.00	57600.00	847.00
10	1/32	11.520	22.917	20.00	230400.00	57600.00	872.00

3.10 Example Frame Descriptor Configuration

This section provides as an example, an OFDM Frame Format using TDD. Sample DCD, UCD, DL-MAP, and UL-MAP are used to provide an example on the construction of Tx and Rx frame descriptors used at the Base Station and Subscriber Station.

Note	Only those parameters in the DL-MAP, UL-MAP, DCD, and UCD messages, relevant to creating Tx and Rx Frame Descriptors, are provided in these examples.

The following system characteristics are assumed in these examples:

- CP size: 1/16
- Channel BW: 3.5 MHz

DCD Channel Encoding	
Change Count	141
TTG	50
RTG	50
BS ID	0x20, 0x30, 0x40, 0x10, 0x02, 0x96
Frame Duration Code	4
Frame Number	314562

Downlink Burst Profile Encodings		
DIUC	**FEC Code Type**	**TCS Enable**
1	0	0
2	1	0
3	2	0
4	3	0
5	4	0
6	5	0
7	6	0

Table 26: DCD Channel Encoding

Downlink Frame Prefix Format (DLFP)	
Base_Station_ID	0x6
Frame_Number	0x2
Configuration_Change_Count	0xd
Reserved	0x0

DL Frame Prefix IE		
Rate ID /DIUC	**Preamble Present**	**Length**
1	0	7
3	0	10
4	0	8
5	0	9

Table 27: DLFP

DL-MAP	
DCD Count	141
BS ID	0x20, 0x30, 0x40, 0x10, 0x02, 0x96

DL-MAP IE's			
CID	**DIUC**	**Preamble Present**	**Start Time**
0xffff	6	0	37
0x2872	3	1	46
0xffff	14	0	53

Table 28: DL-MAP

UCD Channel Encoding	
Change Count	38
BW Request Opportunity Size	136
Ranging Request Opportunity Size	1020
Uplink Burst Profile Encodings:	

UIUC	FEC Code Type	TCS Enable
5	0	1
6	0	0
7	1	0
8	2	0
9	3	0
10	4	0
11	5	0
12	6	0

Table 30: UCD Channel Encoding

UL-MAP	
UCD Count	38
Allocation Start Time	3654
UL-MAP IE's	

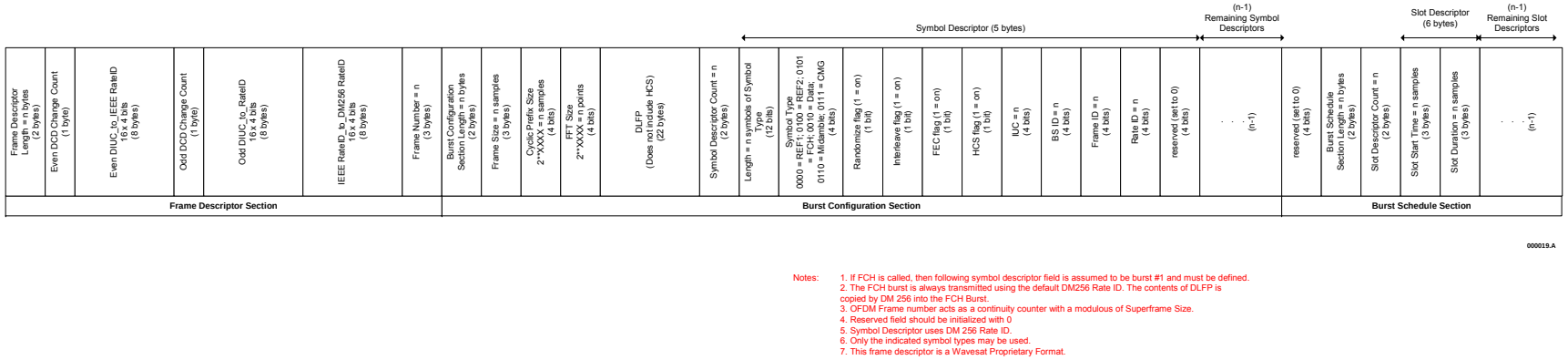
CID	Start Time	Sub Channel Index	UIUC	Duration	Midamble Repetition Interval
0x0000	0	0	1	30	0
0x3912	30	0	8	5	0
0x2377	35	0	9	16	1
0x0000	51	0	14	0	0

Table 29: UL-MAP

3.10.1 General Considerations:

The following are some general considerations to be aware of in this example:

1) Scheduling parameters in the DCD, UCD, and UL- MAP use Physical Slots (PS) as units of timing. The PHY uses units of complex-valued samples or simply, complex samples, where 1 PS = 4 Complex Samples.
2) Given the frame duration code from the DCD Channel Encoding parameters, the size of the frame = 10000 PS or 40000 complex samples, and may contain up to 147 OFDM symbols.
3) Given the CP size = 1/16 from the system characteristics, the size of an OFDM symbol is 68 PS or 272 complex samples. For any given CP size, the symbol duration in complex samples is = 256*(1+ CP_Size), where CP_Size is = ¼, 1/8, 1/16, or 1/32.



Notes:
1. If FCH is called, then following symbol descriptor field is assumed to be burst #1 and must be defined.
2. The FCH burst is always transmitted using the default DM256 Rate ID. The contents of DLFP is copied by DM 256 into the FCH Burst.
3. OFDM Frame number acts as a continuity counter with a modulous of Superframe Size.
4. Reserved field should be initialized with 0
5. Symbol Descriptor uses DM 256 Rate ID.
6. Only the indicated symbol types may be used.
7. This frame descriptor is a Wavesat Proprietary Format.

Figure 15: Linear Representation of Structure of the Frame Descriptor

Also see the larger Figure 7: Structure of the Frame Descriptor. These figures are the same except that one is displayed linearly and the other is displayed for readability.

3.10.2 Programming the Tx Frame Configuration at the Base Station

The Frame Descriptor is broken down into three sections: the Frame Descriptor Section, the Burst Configuration Section, and the Burst Schedule Section. See Figure 15: Linear Representation of Structure of the Frame Descriptor or Figure 7: Structure of the Frame Descriptor. Refer to Section 3.3 Frame Descriptor.

Programming the Tx Frame Descriptor at the Base Station means utilizing the information contained in the DCD, DLFP, and DL-MAP.

3.10.2.1 Frame Descriptor Section

- The Frame Descriptor Length is filled with the value of 173.
- As discussed in an earlier section, the Even DCD Change Count, Even_DIUC_to_IEEE_RateID, Odd DCD Change Count, Odd_DIUC_to_IEEE_RateID, and IEEE_RateID_to_DM256_RateID fields are not used and filled with 0x00.
- The Frame Number field is filled with the value 314562.

See Figure 16: Example Programming the Tx Frame configuration at the Base Station.

3.10.2.2 Burst Configuration Section

- The Burst Configuration Section Length is filled with the value of 78.
- The Frame Size field is filled with the value of 40000.
- The Cyclic Prefix Size field is filled with the value of 4. Thus $2^4 = 16$, indicating to the PHY, the size of the Cyclic Prefix in complex samples.
- The FFT Size field is filled with the value of 8. Thus $2^8 = 256$, indicating to the PHY the size of the FFT. This is the only permitted value.
- The DLFP section is filled exactly according to the example given above in Table 27: DLFP. Unused bytes in this section shall be shall be filled with the value 0x00.

See Figure 16: Example Programming the Tx Frame configuration at the Base Station

- The Symbol Descriptor Count field is filled with the value 10. This means that we are about to describe 10 symbol descriptors as follows:

Symbol Descriptor	Length	Symbol Type	Randomize Flag	Interleave Flag	FEC Flag	HCS Flag	IUC	BS ID	Frame ID	Rate ID	Reserved
1	1	REF1	0	0	0	0	0	0	0	0	0
2	1	REF2	0	0	0	0	0	0	0	0	0
3	1	FCH	1	1	1	1	0	6	2	6	0
4	7	DATA	1	1	1	0	0	6	2	0	0
5	10	DATA	1	1	1	0	3	6	2	1	0
6	8	DATA	1	1	1	0	4	6	2	1	0
7	9	DATA	1	1	1	0	5	6	3	2	0
8	9	DATA	1	1	1	0	6	6	2	4	0
9	1	REF2	0	0	0	0	0	0	0	0	0
10	6	DATA1	1	1	1	0	3	6	2	1	0

Table 31: Symbol Descriptor Information Elements for Programming Tx Frame Configuration at the Base Station Example

See Figure 16: Example Programming the Tx Frame configuration at the Base Station for an example fill of the Symbol Descriptor 1 The Symbol Descriptors 2-10 will follow the example for Symbol Descriptor 1 using Table 31: Symbol Descriptor Information Elements for Programming Tx Frame Configuration at the Base Station Example.

3.10.2.3 Burst Schedule Section

- The Burst Schedule Section Length is filled with the value of 62.

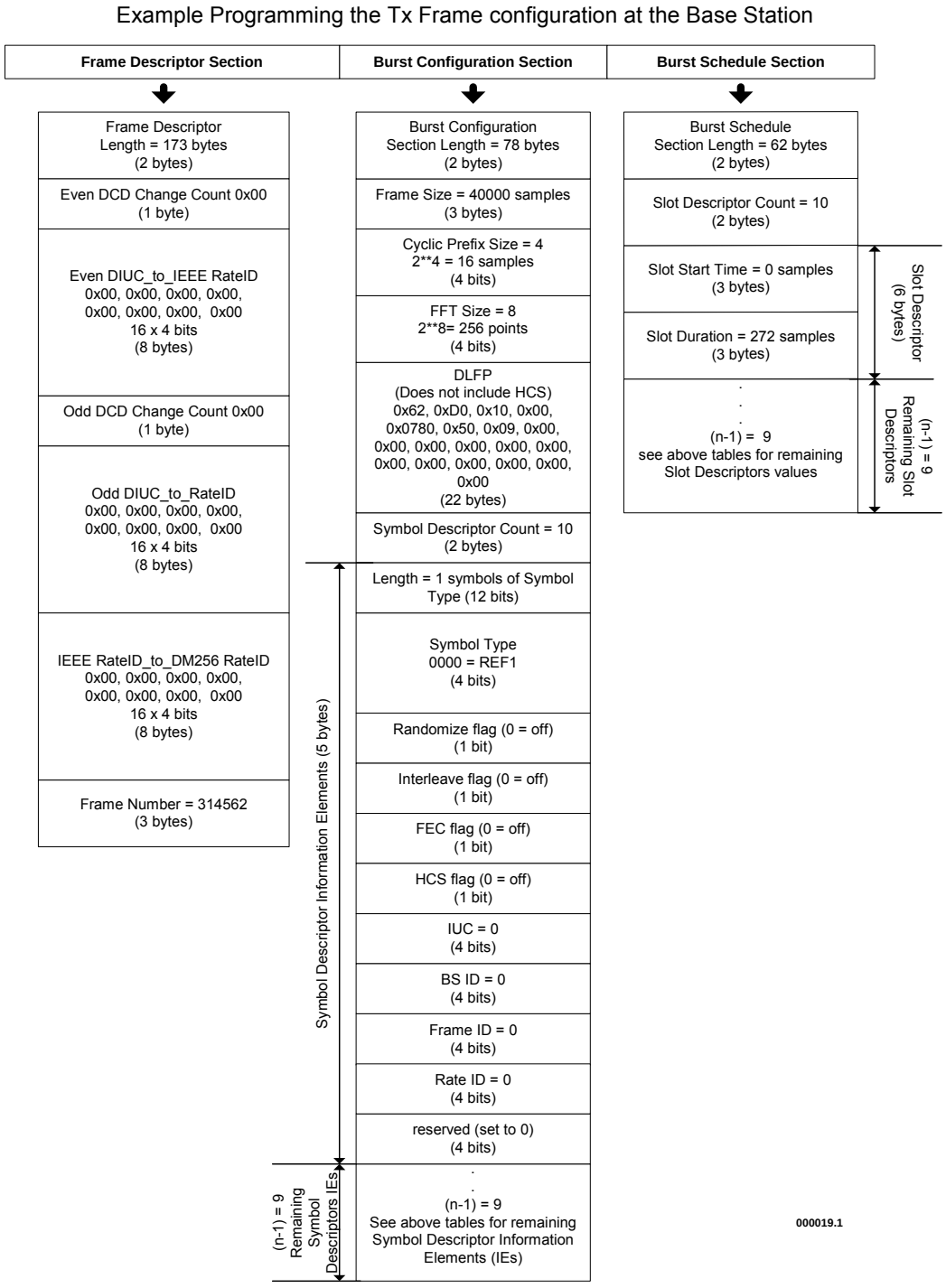
See Figure 16: Example Programming the Tx Frame configuration at the Base Station

- The Slot Descriptor Count is filled with the value of 10, the same as the Symbol Descriptor count. This means that we are about to describe 10 slot descriptors as follows:

Slot Descriptor	Slot Start Time	Slot Duration
1	0	272
2	272	272
3	544	272
4	816	1904
5	2720	2720
6	5440	2176
7	7616	2448
8	10064	2448
9	12512	272
10	12784	1632

Table 32: Slot Descriptor Information Elements for Programming Tx Frame Configuration at the Base Station Example

See Figure 16: Example Programming the Tx Frame configuration at the Base Station for an example fill of the Slot Descriptor 1 The Slot Descriptors 2-10 will follow the example for Slot Descriptor 1 using the Table 32: Slot Descriptor Information Elements for Programming Tx Frame Configuration at the Base Station Example.



Notes:
1. If FCH is called, then following symbol descriptor field is assumed to be burst #1 and must be defined.
2. The FCH burst is always transmitted using the default DM256 Rate ID. The contents of DLFP is copied by DM 256 into the FCH Burst.
3. OFDM Frame number acts as a continuity counter with a modulous of Superframe Size.
4. Reserved field should be initialized with 0
5. Symbol Descriptor uses DM 256 Rate ID.
6. Only the indicated symbol types may be used.
7. This frame descriptor is a Wavesat Proprietary Format.

Figure 16: Example Programming the Tx Frame configuration at the Base Station

3.10.3 Programming the Rx Frame Configuration at the Base Station

The Frame Descriptor is broken down into three sections: the Frame Descriptor Section, the Burst Configuration Section, and the Burst Schedule Section. See Figure 15: Linear Representation of Structure of the Frame Descriptor or Figure 7: Structure of the Frame Descriptor. Refer to Section 3.3 Frame Descriptor.

Programming the Rx Frame Descriptor at the Base Station means utilizing the information contained in the UCD and the UL-MAP.

3.10.3.1 Frame Descriptor Section

- The Frame Descriptor Length is filled with the value of 107.
- As discussed in an earlier section, the Even DCD Change Count, Even_DIUC_to_IEEE_RateID, Odd DCD Change Count, Odd_DIUC_to_IEEE_RateID, and IEEE_RateID_to_DM256_RateID fields are not used and shall be filled with 0x00.
- The Frame Number field is filled with the value 314562.

See Figure 17: Example Programming the Rx Frame configuration at the Base Station.

3.10.3.2 Burst Configuration Section

- The Burst Configuration Section Length is filled with the value of 48.
- The Frame Size field is filled with the value of 40000.
- The Cyclic Prefix Size field is filled with the value of 4. Thus $2^4 = 16$, indicating to the PHY, the size of the Cyclic Prefix in complex samples.
- The FFT Size field is filled with the value of 8. Thus $2^8 = 256$, indicating to the PHY, the size of the FFT. This is the only permitted value.
- The DLFP section shall be filled with 0x00.

See Figure 17: Example Programming the Rx Frame configuration at the Base Station.

- The Symbol Descriptor Count field is filled with the value 4. This means that we are about to describe 4 symbol descriptors as follows:

Symbol Descriptor	Length	Symbol Type	Randomize Flag	Interleave Flag	FEC Flag	HCS Flag	IUC	BS ID	Frame ID	Rate ID	Reserved
1	2	DATA	1	1	1	0	1	6	2	0	0
2	2	DATA	1	1	1	0	1	6	2	0	0
3	4	DATA	1	1	1	0	8	6	2	1	0
4	13	DATA	1	1	1	0	9	6	2	2	0

Table 33: Symbol Descriptor Information Elements for Programming Rx Frame Configuration at the Base Station Example

See Figure 17: Example Programming the Rx Frame configuration at the Base Station for an example fill of the Symbol Descriptor 1 The Symbol Descriptors 2-4 will follow the example for Symbol Descriptor 1 using Table 33: Symbol Descriptor Information Elements for Programming Rx Frame Configuration at the Base Station Example.

3.10.3.3 Burst Schedule Section

- The Burst Schedule Section Length is filled with the value of 26.

See Figure 17: Example Programming the Rx Frame configuration at the Base Station.

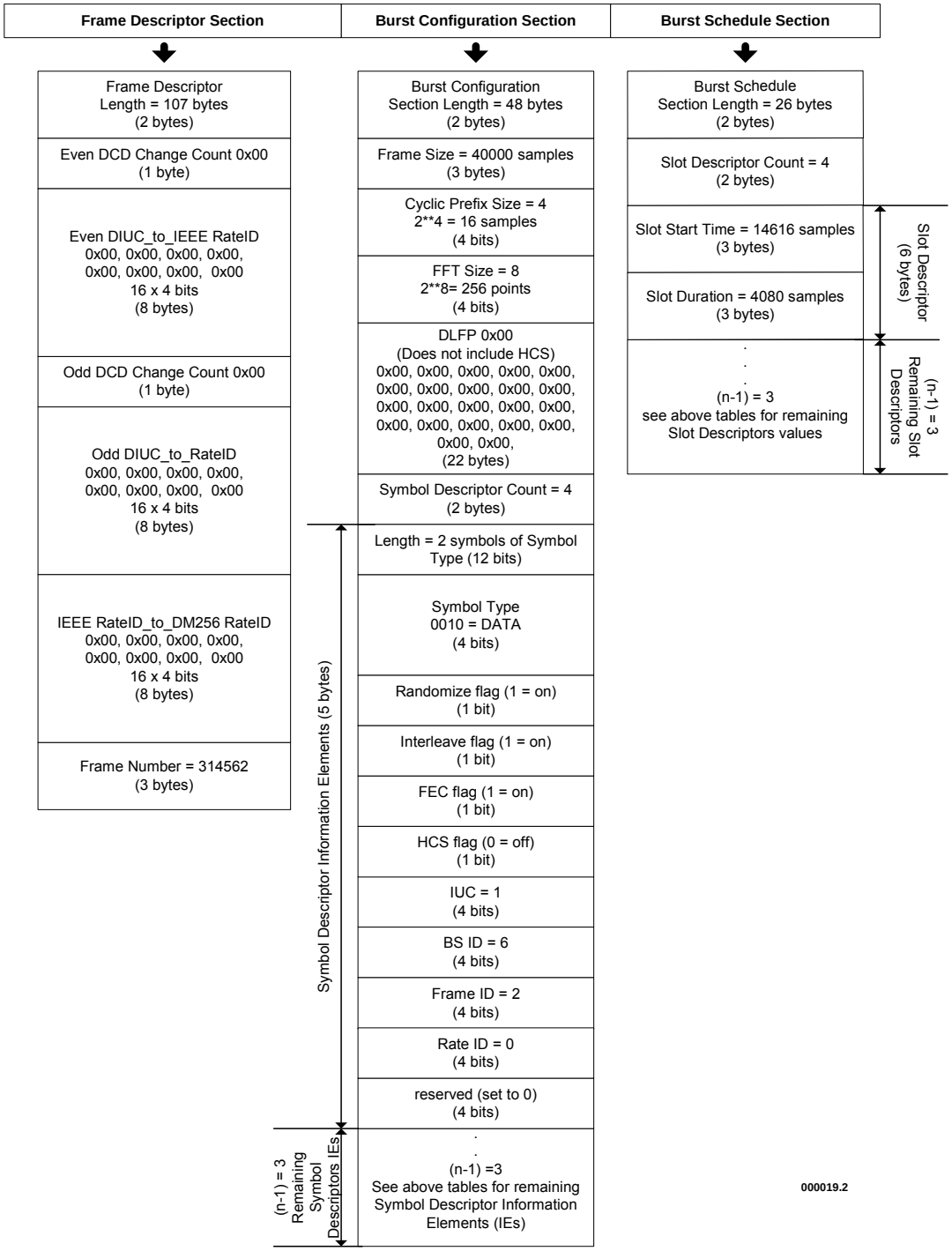
- The Slot Descriptor Count is filled with the value of 4, the same as the Symbol Descriptor count. This means that we are about to describe 4 slot descriptors as follows:

Slot Descriptor	Slot Start Time	Slot Duration
1	14616	4080
2	18696	4080
3	22776	1360
4	24136	4352

Table 34: Slot Descriptor for Programming Rx Frame Configuration at the Base Station Example

See Figure 17: Example Programming the Rx Frame configuration at the Base Station for an example fill of the Slot Descriptor 1 The Slot Descriptors 2-4 will follow the example for Slot Descriptor 1 using Table 34: Slot Descriptor for Programming Rx Frame Configuration at the Base Station Example.

Example Programming the Rx Frame configuration at the Base Station



Notes:
1. If FCH is called, then following symbol descriptor field is assumed to be burst #1 and must be defined.
2. The FCH burst is always transmitted using the default DM256 Rate ID. The contents of DLFP is copied by DM 256 into the FCH Burst.
3. OFDM Frame number acts as a continuity counter with a modulous of Superframe Size.
4. Reserved field should be initialized with 0
5. Symbol Descriptor uses DM 256 Rate ID.
6. Only the indicated symbol types may be used.
7. This frame descriptor is a Wavesat Proprietary Format.

Figure 17: Example Programming the Rx Frame configuration at the Base Station

3.10.4 Programming the Rx Frame Configuration at the Subscriber Station

The Frame Descriptor is broken down into three sections: the Frame Descriptor Section, the Burst Configuration Section, and the Burst Schedule Section. See Figure 15: Linear Representation of Structure of the Frame Descriptor or Figure 7: Structure of the Frame Descriptor. Refer to Section 3.3 Frame Descriptor.

Programming the Rx Frame Descriptor at the Subscriber Station means utilizing the information contained in the DCD and the DL-MAP.

Specific Considerations:

1) Since the subscriber station's frame count is free running, the frame number used in the Frame Descriptor Section is that value which is contained in the PHY's frame number register. For this example, assume the contents of this register read 0x1234 when the DL-MAP is received.
2) All subscriber station's which have synchronized to the DL should program their Rx Frame Descriptors to receive the bursts not decoded by the DLFP.

3.10.4.1 Frame Descriptor Section

- The Frame Descriptor Length is filled with the value of 85.

Figure 18: Example Programming the Rx Frame configuration at the Subscriber Station

- As discussed in an earlier section, the Even DCD Change Count, Even_DIUC_to_IEEE_RateID, Odd DCD Change Count, Odd_DIUC_to_IEEE_RateID, and IEEE_RateID_to_DM256_RateID fields are used at the Subscriber Station. These structures are filled as follows:

Even DCD Change Count								140							
Even DIUC_to_IEEE_RateID															
Value	0xf	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0xe	0xe	0xe	0xe	0xe	0xd	0xf	0xf
Byte Offset	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Odd DCD Change Count								139							
Odd DIUC_to_IEEE_RateID															
Value	0xf	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0xe	0xe	0xe	0xe	0xe	0xd	0xf	0xf
Byte Offset	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
IEEE RateID_to_DM256RateID																
Value	0x6	0x0	0x1	0x2	0x3	0x4	0x5	0xe	0xe	0xe	0xe	0xe	0xe	0xd	0xf	0xf
Byte Offset	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Table 35: Frame Descriptor Information Elements for Programming Rx Frame Configuration at the Subscriber Station Example

See Figure 18: Example Programming the Rx Frame configuration at the Subscriber Station for an example fill of the Frame Descriptor using Table 35: Frame Descriptor Information Elements for Programming Rx Frame Configuration at the Subscriber Station Example.

- The Frame Number field is filled with the value 0x1234.

Figure 18: Example Programming the Rx Frame configuration at the Subscriber Station

3.10.4.2 Burst Configuration Section

- The Burst Configuration Section Length is filled with the value of 38.
- The Frame Size field is filled with the value of 40000.
- The Cyclic Prefix Size field is filled with the value of 4. Thus $2^4 = 16$, indicating to the PHY, the size of the Cyclic Prefix in complex samples.
- The FFT Size field is filled with the value of 8. Thus $2^8 = 256$, indicating to the PHY, the size of the FFT. This is the only permitted value.
- The DLFP section shall be filled with the value 0x00.

Figure 18: Example Programming the Rx Frame configuration at the Subscriber Station

- The Symbol Descriptor Count field is filled with the value 2, which will define the two DL-MAP IE's that we received. The 2 symbol descriptors are as follows:

Symbol Descriptor	Length	Symbol Type	Randomize Flag	Interleave Flag	FEC Flag	HCS Flag	IUC	BS ID	Frame ID	Rate ID	Reserved
1	9	DATA	1	1	1	0	6	6	2	4	0
2	6	DATA	1	1	1	0	3	6	2	12	0

Table 36: Symbol Descriptor Information Elements for Programming Rx Frame Configuration at the Subscriber Station Example

See Figure 18: Example Programming the Rx Frame configuration at the Subscriber Station for an example fill of the Symbol Descriptor 1 The Symbol Descriptors 2 will follow the example for Symbol Descriptor 1 using Table 36: Symbol Descriptor Information Elements for Programming Rx Frame Configuration at the Subscriber Station Example.

3.10.4.3 Burst Schedule Section

- The Burst Schedule Section Length is filled with the value of 14.

Figure 18: Example Programming the Rx Frame configuration at the Subscriber Station

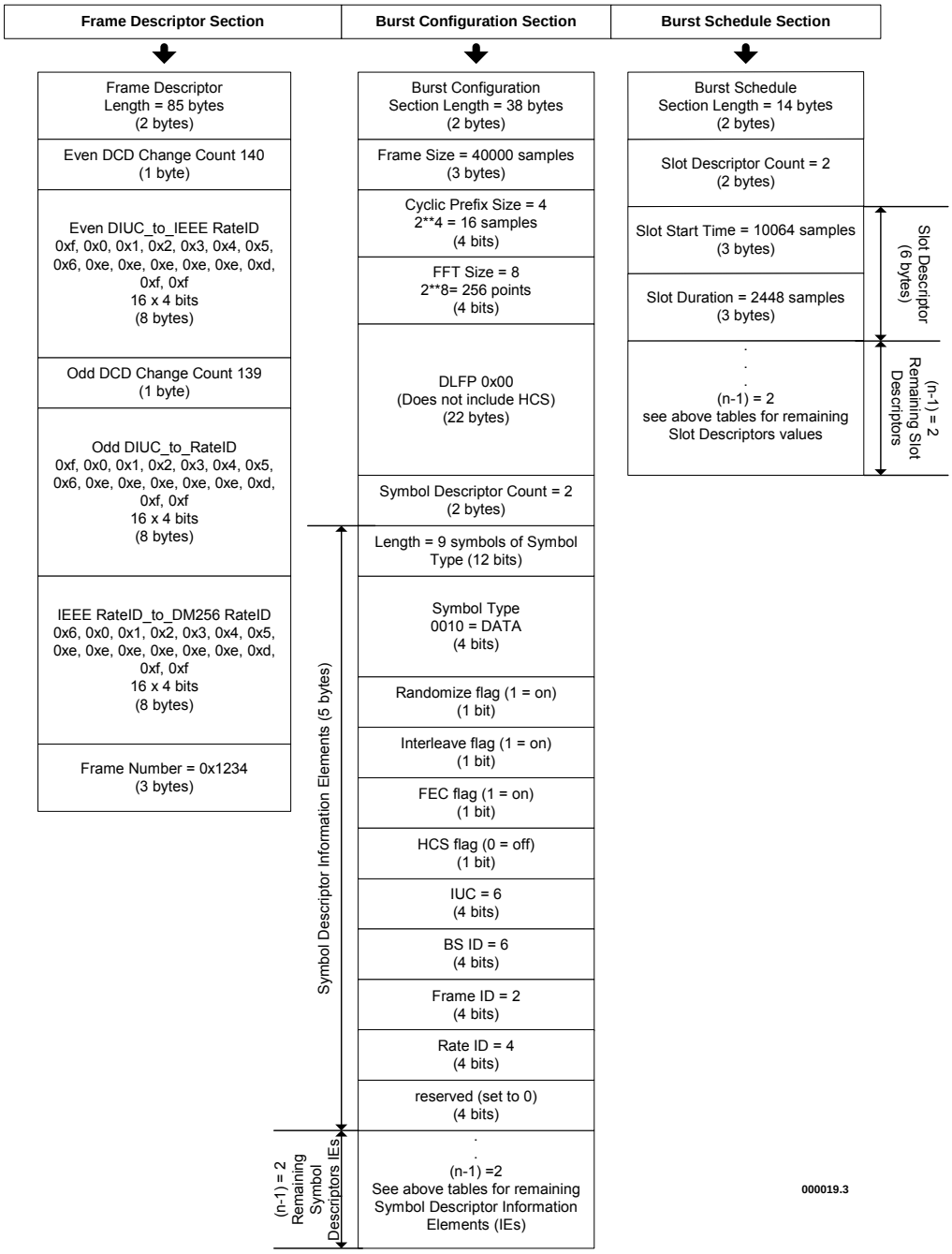
- The Slot Descriptor Count is filled with the value of 2, the same as the Symbol Descriptor count and the number of DL-MAP IE's. The 2 slot descriptors are as follows:

Slot Descriptor	Slot Start Time	Slot Duration
1	10064	2448
2	12512	1904

Table 37: Slot Descriptor Information Elements for Programming Rx Frame Configuration at the Subscriber Station Example

See Figure 18: Example Programming the Rx Frame configuration at the Subscriber Station for an example fill of the Slot Descriptor using Table 37: Slot Descriptor Information Elements for Programming Rx Frame Configuration at the Subscriber Station Example.

Example Programming the Rx Frame configuration at the Subscriber Station



Notes:
1. If FCH is called, then following symbol descriptor field is assumed to be burst #1 and must be defined.
2. The FCH burst is always transmitted using the default DM256 Rate ID. The contents of DLFP is copied by DM 256 into the FCH Burst.
3. OFDM Frame number acts as a continuity counter with a modulous of Superframe Size.
4. Reserved field should be initialized with 0
5. Symbol Descriptor uses DM 256 Rate ID.
6. Only the indicated symbol types may be used.
7. This frame descriptor is a Wavesat Proprietary Format.

Figure 18: Example Programming the Rx Frame configuration at the Subscriber Station

3.10.5 Programming the Tx Frame Configuration at Subscriber Station #1

The Frame Descriptor is broken down into three sections: the Frame Descriptor Section, the Burst Configuration Section, and the Burst Schedule Section. See Figure 15: Linear Representation of Structure of the Frame Descriptor or Figure 7: Structure of the Frame Descriptor. Refer to Section 3.3 Frame Descriptor.

Programming the Tx Frame Descriptor at the Subscriber Station means utilizing the information contained in the UCD and the UL-MAP.

Specific Considerations:

1) Since the subscriber station's frame count is free running, the frame number used in the Frame Descriptor Section is that value which is contained in the PHY's frame number register. For this example, assume the contents of this register read 0x1003 when the UL-MAP is received. Since the allocation start time in the UL-MAP is less than the value of for the given frame size (10000 PS), the allocation is for the current frame.
2) In this example, we assume that this subscriber is in the process of Initial Ranging and has no Basic CID assigned. Therefore, this subscriber makes use of one of the two Initial Ranging opportunities provided in the UL-MAP to make an Initial Ranging Request. For this example, the subscriber chooses transmission opportunity number 2.

3.10.5.1 Frame Descriptor Section

- The Frame Descriptor Length is filled with the value of 96.
- As discussed in an earlier section, the Even DCD Change Count, Even_DIUC_to_IEEE_RateID, Odd DCD Change Count, Odd_DIUC_to_IEEE_RateID, and IEEE_RateID_to_DM256_RateID fields is not used in transmission at the Subscriber Station and shall be filled with 0x00.
- The Frame Number field is filled with the value 0x1003.

See Figure 19: Example Programming the Tx Frame configuration at the Subscriber Station #1.

3.10.5.2 Burst Configuration Section

- The Burst Configuration Section Length is filled with the value of 43.
- The Frame Size field is filled with the value of 40000.
- The Cyclic Prefix Size field is filled with the value of 4. Thus $2^4 = 16$, indicating to the PHY, the size of the Cyclic Prefix in complex samples.
- The FFT Size field is filled with the value of 8. Thus $2^8 = 256$, indicating to the PHY, the size of the FFT. This is the only permitted value.
- The DLFP section shall be filled with the value 0x00.

See Figure 19: Example Programming the Tx Frame configuration at the Subscriber Station #1.

The Symbol Descriptor Count field is filled with the value 3, which is used to define the long preamble and the most robust mandatory profile needed to carry the Initial Ranging Request. The 3 symbol descriptors are as follows:

Symbol Descriptor	Length	Symbol Type	Randomize Flag	Interleave Flag	FEC Flag	HCS Flag	IUC	BS ID	Frame ID	Rate ID	Reserved
1	1	REF1	0	0	0	0	0	0	0	0	0
2	1	REF2	0	0	0	0	0	0	0	0	0
3	2	DATA	1	1	1	0	1	6	2	6	0

Table 38: Symbol Descriptor Information Elements for Programming Tx Frame Configuration at the Subscriber Station #1 Example

See Figure 19: Example Programming the Tx Frame configuration at the Subscriber Station #1 for an example fill of the Symbol Descriptor using Table 38: Symbol Descriptor Information Elements for Programming Tx Frame Configuration at the Subscriber Station #1 Example.

3.10.5.3 Burst Schedule Section

- The Burst Schedule Section Length is filled with the value of 20.

See Figure 19: Example Programming the Tx Frame configuration at the Subscriber Station #1.

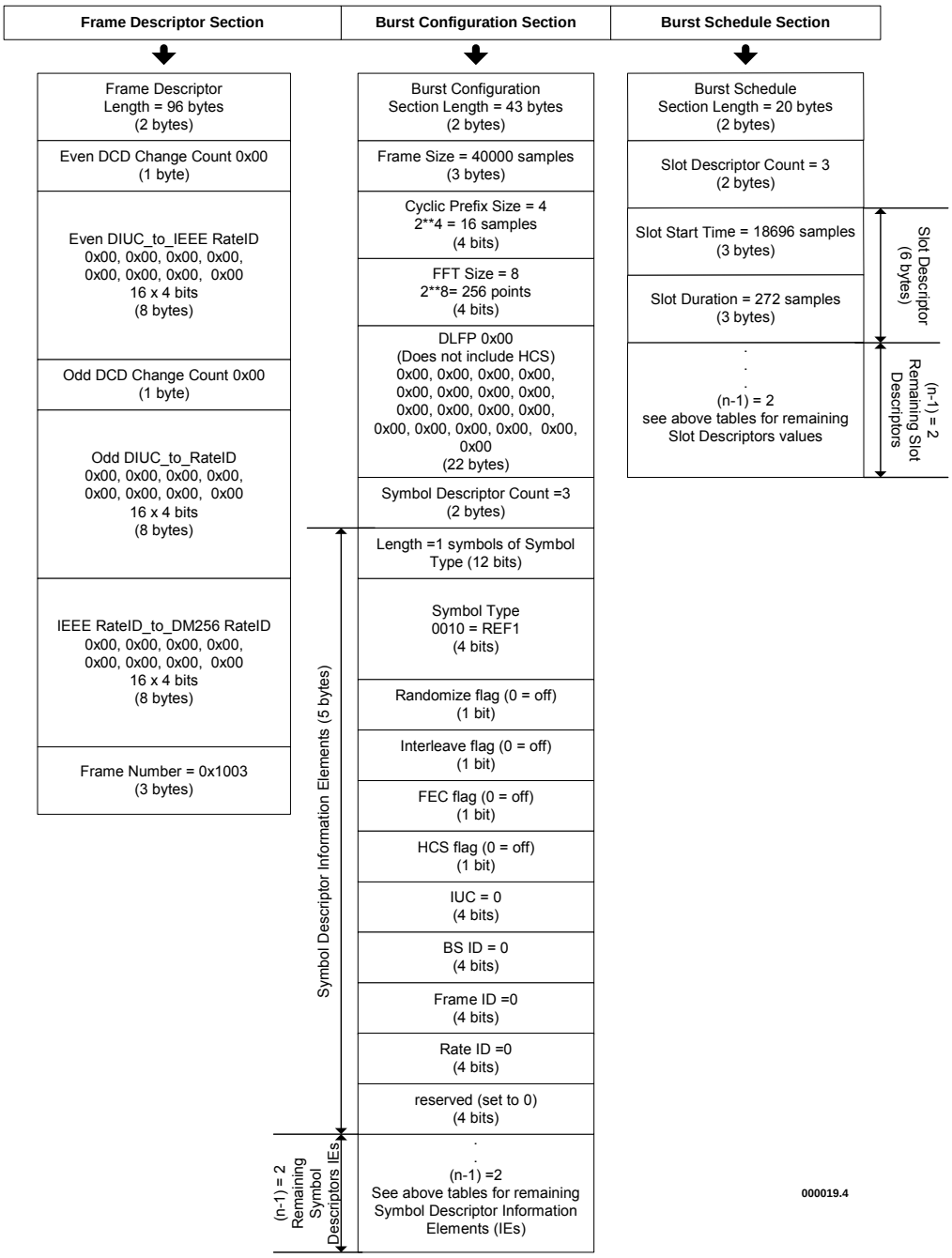
The Slot Descriptor Count is filled with the value of 3, the same as the Symbol Descriptor count. The 3 slot descriptors are as follows:

Slot Descriptor	Slot Start Time	Slot Duration
1	18696	272
2	18968	272
3	19240	544

Table 39: Slot Descriptor Information Elements for Programming Tx Frame Configuration at the Subscriber Station #1 Example

See Figure 19: Example Programming the Tx Frame configuration at the Subscriber Station #1 for an example fill of the Slot Descriptor using .Table 39: Slot Descriptor Information Elements for Programming Tx Frame Configuration at the Subscriber Station #1 Example

Example Programming the Tx Frame configuration at the Subscriber Station #1



Notes:
1. If FCH is called, then following symbol descriptor field is assumed to be burst #1 and must be defined.
2. The FCH burst is always transmitted using the default DM256 Rate ID. The contents of DLFP is copied by DM 256 into the FCH Burst.
3. OFDM Frame number acts as a continuity counter with a modulous of Superframe Size.
4. Reserved field should be initialized with 0
5. Symbol Descriptor uses DM 256 Rate ID.
6. Only the indicated symbol types may be used.
7. This frame descriptor is a Wavesat Proprietary Format.

Figure 19: Example Programming the Tx Frame configuration at the Subscriber Station #1

3.10.6 Example Programming the Tx Frame configuration at the Subscriber Station #2

The Frame Descriptor is broken down into three sections: the Frame Descriptor Section, the Burst Configuration Section, and the Burst Schedule Section. See Figure 15: Linear Representation of Structure of the Frame Descriptor or Figure 7: Structure of the Frame Descriptor. Refer to Section 3.3 Frame Descriptor.

Programming the Tx Frame Descriptor at the Subscriber Station means utilizing the information contained in the UCD and the UL-MAP.

Specific Considerations:

1) Since the subscriber station's frame count is free running, the frame number used in the Frame Descriptor Section is that value which is contained in the PHY's frame number register. For this example, assume the contents of this register read 0x1234 when the UL-MAP is received. Since the allocation start time in the UL-MAP is less than the value of for the given frame size (10000 PS), the allocation is for the current frame.
2) In this example, we assume that this subscriber is ranged and is assigned a Basic CID = 0x3912

3.10.6.1 Frame Descriptor Section

- The Frame Descriptor Length is filled with the value of 85.
- As discussed in an earlier section, the Even DCD Change Count, Even_DIUC_to_IEEE_RateID, Odd DCD Change Count, Odd_DIUC_to_IEEE_RateID, and IEEE_RateID_to_DM256_RateID fields is not used in transmission at the Subscriber Station and shall be filled with 0x00.
- The Frame Number field is filled with the value 0x1234.

See Figure 20: Example Programming the Tx Frame configuration at the Subscriber Station #2

3.10.6.2 Burst Configuration Section

- The Burst Configuration Section Length is filled with the value of 38.
- The Frame Size field is filled with the value of 40000.
- The Cyclic Prefix Size field is filled with the value of 4. Thus $2^4 = 16$, indicating to the PHY, the size of the Cyclic Prefix in complex samples.
- The FFT Size field is filled with the value of 8. Thus $2^8 = 256$, indicating to the PHY, the size of the FFT. This is the only permitted value.
- The DLFP section shall be filled with the value 0x00.

See Figure 20: Example Programming the Tx Frame configuration at the Subscriber Station #2

- The Symbol Descriptor Count field is filled with the value 2, which is used to define the short preamble and the burst profile associated with the CID. The 2 symbol descriptors are as follows:

Symbol Descriptor	Length	Symbol Type	Randomize Flag	Interleave Flag	FEC Flag	HCS Flag	IUC	BS ID	Frame ID	Rate ID	Reserved
1	1	REF2	0	0	0	0	0	0	0	0	0
2	4	DATA	1	1	1	0	8	6	2	1	0

Table 40: Symbol Descriptor Information Elements for Programming Tx Frame Configuration at the Subscriber Station #2 Example

See Figure 20: Example Programming the Tx Frame configuration at the Subscriber Station #2 for an example fill of the Symbol Descriptor using Table 40: Symbol Descriptor Information Elements for Programming Tx Frame Configuration at the Subscriber Station #2 Example.

Burst Schedule Section

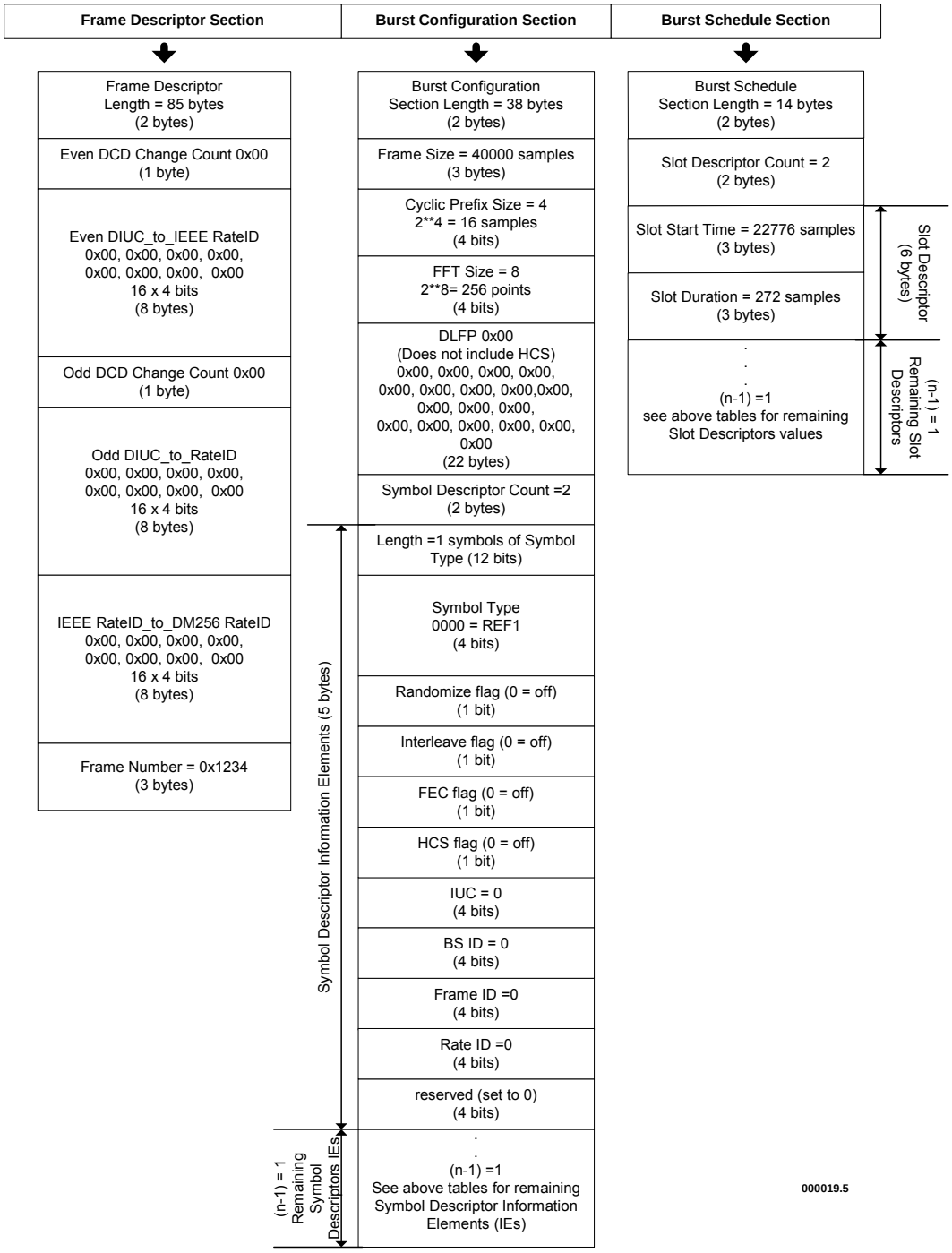
- The Burst Schedule Section Length is filled with the value of 14.
- The Slot Descriptor Count is filled with the value of 2, the same as the Symbol Descriptor count. The 2 slot descriptors are as follows:

Slot Descriptor	Slot Start Time	Slot Duration
1	22776	272
2	23048	1088

Table 41: Slot Descriptor Information Elements for Programming Tx Frame Configuration at the Subscriber Station #2 Example

See Figure 20: Example Programming the Tx Frame configuration at the Subscriber Station #2 for an example fill of the Slot Descriptor using .Table 41: Slot Descriptor Information Elements for Programming Tx Frame Configuration at the Subscriber Station #2 Example

Example Programming the Tx Frame configuration at the Subscriber Station #2



Notes:
1. If FCH is called, then following symbol descriptor field is assumed to be burst #1 and must be defined.
2. The FCH burst is always transmitted using the default DM256 Rate ID. The contents of DLFP is copied by DM 256 into the FCH Burst.
3. OFDM Frame number acts as a continuity counter with a modulous of Superframe Size.
4. Reserved field should be initialized with 0
5. Symbol Descriptor uses DM 256 Rate ID.
6. Only the indicated symbol types may be used.
7. This frame descriptor is a Wavesat Proprietary Format.

Figure 20: Example Programming the Tx Frame configuration at the Subscriber Station #2

3.10.7 Programming the Tx Frame Configuration at Subscriber Station #3

The Frame Descriptor is broken down into three sections: the Frame Descriptor Section, the Burst Configuration Section, and the Burst Schedule Section. See Figure 15: Linear Representation of Structure of the Frame Descriptor or Figure 7: Structure of the Frame Descriptor. Refer to Section 3.3 Frame Descriptor.

Programming the Tx Frame Descriptor at the Subscriber Station means utilizing the information contained in the UCD and the UL-MAP.

Specific Considerations:

1) Since the subscriber station's frame count is free running, the frame number used in the Frame Descriptor Section is that value which is contained in the PHY's frame number register. For this example, assume the contents of this register read 0x3114 when the UL-MAP is received. Since the allocation start time in the UL-MAP is less than the value of for the given frame size (10000 PS), the allocation is for the current frame.
2) In this example, we assume that this subscriber is ranged and is assigned a Basic CID = 0x2377. Since the use of mid-ambles is indicated in the UL-MAP IE for this CID, several symbol and slot descriptors are required.

3.10.7.1 Frame Descriptor Section

- The Frame Descriptor Length is filled with the value of 118.
- As discussed in an earlier section, the Even DCD Change Count, Even_DIUC_to_IEEE_RateID, Odd DCD Change Count, Odd_DIUC_to_IEEE_RateID, and IEEE_RateID_to_DM256_RateID fields is not used in transmission at the Subscriber Station and shall be filled with 0x00.
- The Frame Number field is filled with the value 0x3114.

See Figure 21: Example Programming the Tx Frame configuration at the Subscriber Station #3.

3.10.7.2 Burst Configuration Section

- The Burst Configuration Section Length is filled with the value of 53.
- The Frame Size field is filled with the value of 40000.
- The Cyclic Prefix Size field is filled with the value of 4. Thus $2^4 = 16$, indicating to the PHY, the size of the Cyclic Prefix in complex samples.
- The FFT Size field is filled with the value of 8. Thus $2^8 = 256$, indicating to the PHY, the size of the FFT. This is the only permitted value.
- The DLFP section shall be filled with the value 0x00.

See Figure 21: Example Programming the Tx Frame configuration at the Subscriber Station #3.

- The Symbol Descriptor Count field is filled with the value 5, which is the number of descriptors required to define the short preamble, mid-amble, post-amble and data symbols of the UL burst associated with the CID 0x2377. The 5 symbol descriptors are as follows:

Symbol Descriptor	Length	Symbol Type	Randomize Flag	Interleave Flag	FEC Flag	HCS Flag	IUC	BS ID	Frame ID	Rate ID	Reserved
1	1	REF2	0	0	0	0	0	0	0	0	0
2	8	DATA	1	1	1	0	9	6	2	2	0
3	1	MIDAMBLE	0	0	0	0	0	0	0	0	0
4	5	DATA	1	1	1	0	9	6	2	2	0
5	1	REF2	0	0	0	0	0	0	0	0	0

Table 42: Symbol Descriptor Information Elements for Programming Tx Frame Configuration at the Subscriber Station #3 Example

See Figure 21: Example Programming the Tx Frame configuration at the Subscriber Station #3 for an example fill of the Symbol Descriptor using Table 42: Symbol Descriptor Information Elements for Programming Tx Frame Configuration at the Subscriber Station #3 Example.

3.10.7.3 Burst Schedule Section

- The Burst Schedule Section Length is filled with the value of 32.

See Figure 21: Example Programming the Tx Frame configuration at the Subscriber Station #3.

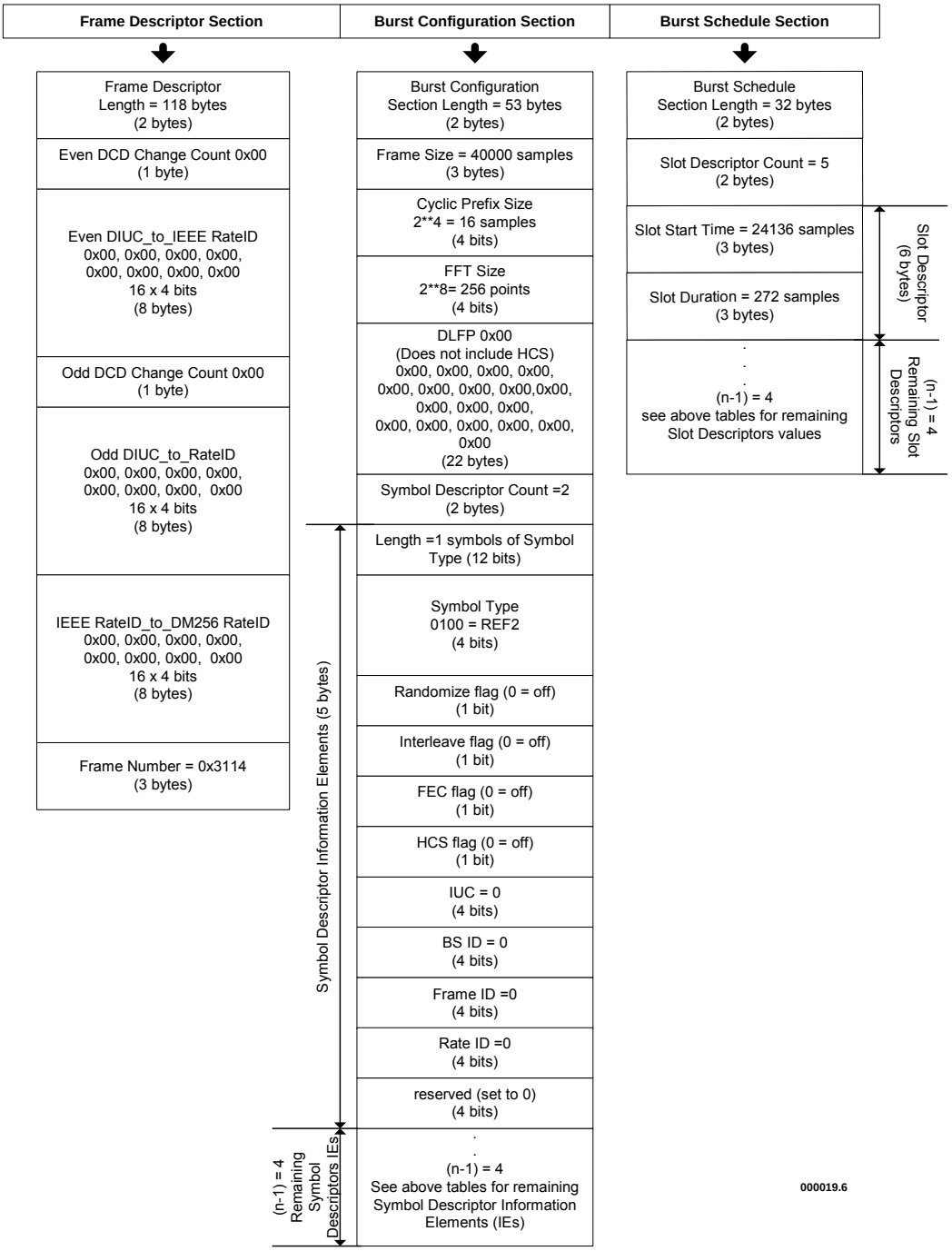
- The Slot Descriptor Count is filled with the value of 5, the same as the Symbol Descriptor count. The 5 slot descriptors are as follows:

Slot Descriptor	Slot Start Time	Slot Duration
1	24136	272
2	24408	2176
3	26584	272
4	26856	1360
5	28216	272

Table 43: Slot Descriptor Information Elements for Programming Tx Frame Configuration at the Subscriber Station #2 Example

See Figure 21: Example Programming the Tx Frame configuration at the Subscriber Station #3 for an example fill of the Slot Descriptor using Table 43: Slot Descriptor Information Elements for Programming Tx Frame Configuration at the Subscriber Station #2 Example.

Example Programming the Tx Frame configuration at the Subscriber Station #3



Notes:
1. If FCH is called, then following symbol descriptor field is assumed to be burst #1 and must be defined.
2. The FCH burst is always transmitted using the default DM256 Rate ID. The contents of DLFP is copied by DM 256 into the FCH Burst.
3. OFDM Frame number acts as a continuity counter with a modulous of Superframe Size.
4. Reserved field should be initialized with 0
5. Symbol Descriptor uses DM 256 Rate ID.
6. Only the indicated symbol types may be used.
7. This frame descriptor is a Wavesat Proprietary Format.

Figure 21: Example Programming the Tx Frame configuration at the Subscriber Station #3

3.11 Frame Transmission and Reception

The MAC Layer must set the one of the following control bits after it has written to a configuration buffer. Setting one of those bits initiates the transmission of a frame or a burst, or its reception, based on the content of the corresponding Frame Configuration buffer.

Tx Frame Configuration Buffer 1 Ready.
Rx Frame Configuration Buffer 1 Ready.
Tx Frame Configuration Buffer 2 Ready.
Rx Frame Configuration Buffer 2 Ready.

DM 256 triggers one of the following interrupts when it has completed the transmission or reception of a frame:

End of Tx Frame interrupt.
Start of REF2.

3.12 Statistical Header Description

A Statistical Header is prepended to every symbol received by the DM 256. The Statistical Header describes the conditions in which the symbol was received, such as the length of symbol. The Figure 22: Statistical Header describes the contents of the Statistical Header.

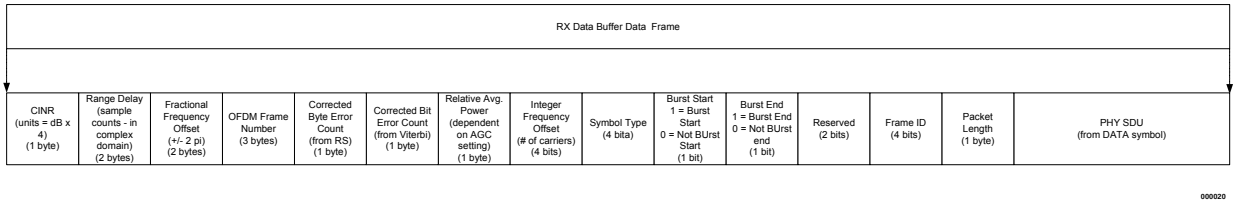


Figure 22: Statistical Header

3.12.1 CINR

The carrier-to-interference-and-noise ratio of the received symbol is multiplied by four.

3.12.2 Range Offset

The Range Offset is the timing difference in complex samples between when the first sample of the first symbol in a burst is received at the Base Station and when the Base Station expected to receive that symbol. This timing difference is due to the physical distance of the Base Station and the Subscriber Station, causing a round-trip propagation delay. This value is used in a Ranging-Response (RNG-RSP) message from the Base Station to the Subscriber Station, indicating how much the Subscriber Station should advance its transmission to appear co-located by the Base Station.

3.12.3 OFDM Frame Number

The DM 256 always starts its Frame Number at zero on power-up and increments this value every frame. However, since the Subscriber Station might be powered on at a different time than the Base Station, its local OFDM Frame Number will be offset from the reference Base Station's local OFDM Frame Number. This field with in the Statistical Header specifies the local OFDM Frame Number in which the symbol was received. Note the difference between OFDM Frame Number and Frame ID. Hence, at the Base Station, the least significant 4 bits of OFDM Frame Number will always be the same as the Frame ID. While at the Subscriber Station, Frame ID is the value that was carried in the DLFP when it is transmitted from the Base Station. Its value is consistent throughout the current frame. OFDM Frame Number is used at the Subscriber Station for scheduling transmission of UL bursts relative to the current OFDM Frame Number.

3.12.4 Corrected RS Bits Count

- For Data Payload: the number of bits corrected by the Reed-Solomon decoder.
- For all other payload: Reed-Solomon does not apply and this field contains 0xFF.

3.12.5 Corrected Bit Error Count

- For Data Payload: the number of Viterbi decoding bit corrections applied to the subsequent payload.
- For all other payload: Viterbi does not apply and the field defaults to 0xFF.

3.12.6 Relative Average Power

This value, ranging from 0 to 255, and indicates the average relative power measurement of a symbol. The value can be converted to an uncalibrated dB value using the following equation.

$$Power(dB) = 10\log(Average\,\mathrm{Re}\,lativePower)$$

This can be used by the Base Station's MAC to indicate to the transmitting Subscriber whether the power level is sufficient (or excessive) via a Ranging Response (RNG-RSP) message.

3.12.7 Fractional Frequency Offset and Integer Frequency Offset

These two fields are used to calculate the overall Frequency Offset. Note that when the AFC is enabled, the overall Frequency Offset is automatically compensated for. Otherwise, is can be used by the Base Station to inform a Subscriber via a RNG-RSP message that a Frequency Correction must be performed. The formula to calculate the overall Frequency Offset is:

$$\Delta f = \left(\frac{\varepsilon_{frac}}{2^{15}} + k_{\mathrm{int}} \right) \frac{f_{s\_bb}}{256}$$

where:

ε_{frac} = Fractional Frequency Offset

k_{int} = Integer Frequency Offset

f_{s_bb} = Baseband Sampling Frequency

Table 44: Baseband Sampling Frequency

Channel Bandwidth	Baseband Sampling Frequency
1.75 MHz	2 MHz
3.5 MHz	4 MHz
7 MHz	8 MHz
10 MHz	11.52 MHz

3.12.8 Symbol Type

The symbol type that these statistics apply to

Symbol Type	Description
0	REF1
1	Reserved
2	Data Payload
3	Reserved
4	REF2
5	FCH
6	Midamble
7	Gap
8-15	Reserved

3.12.9 Burst Start

A value of 1 indicates that this symbol is the first symbol in the burst.

3.12.10 Burst End

A value of 1 indicates that this symbol is the last symbol in the burst

3.12.11 Frame ID

The reference Frame ID that the symbol was received on. It corresponds to the Frame ID field in the DLFP. This field is used for seeding the randomizer for DL and UL bursts.

3.12.12 Packet Length

The Packet Length is the size in bytes of the uncoded block size that follows.

3.12.13 Interpreting the Statistics in the Statistical header

The MAC Layer has several choices in interpreting the statistics of a MAC PDU that spans several OFDM Symbols depending on the degree of inspection desired:

Methods	Description
1	Apply the statistics in the first statistical header that applies in the MAC Header. ***(Wavesat Recommended Method)***
2	Average out the statistics in all the statistical headers that apply in the MAC Header.
3	Apply the statistics in the first statistical header that applies in the Payload.
4	Average out the statistics in all the statistical headers that apply in the Payload.
5	Average out the statistics in all the statistical headers.
6	Pick one of the statistical headers for the MAC PDU at random.

There are many other options but IEEE802.16-2004 does not specify any particular method of interpreting the Statistics at the Base Station. Wavesat recommends that Method 1 be used because of its simplicity and the Statistical values should not vary greatly from OFDM Symbol to OFDM Symbol in a single MAC PDU.

3.13 AFC, ALC and AGC Descriptions

DM256 provides Automatic Frequency Correction (AFC) to compensate for any discrepancy in frequency between a Subscriber Station and the Base Station. The AFC is connected to the Voltage Control (VC) pin of the 10MHz VCTCXO (Voltage Controlled Temperature Compensated Crystal Oscillator).

DM256 provides Automatic Level Control and Automatic Gain Control to compensate for the signal loss caused by distance separation between a Subscriber Station and the Base Station. Both ALC and AGC are performed at the Subscriber Station.

	ASIC / FPGA When external DACs are used via the SPI interface				ASIC When built in DACs are used			
	UL		DL		UL		DL	
	BS rx_bs_1_ss_0 = 1	SS tx_bs_1_ss_0 = 0	BS tx_bs_1_ss_0 = 1	SS rx_bs_1_ss_0 = 0	BS rx_bs_1_ss_0 = 1	SS tx_bs_1_ss_0 = 0	BS tx_bs_1_ss_0 = 1	SS rx_bs_1_ss_0 = 0
AFC				√ (2)				√ (2)
AGC	√ (1) special test			√ (2)				√ (2) √ (3)
ALC		√ (2)				√ (2)		

(1): For test purpose only (should not be enabled in regular operating mode). Value will be refreshed with AGC unit value when a good OFDM symbol is received. (When gets an "rx_ofdm_frame" from the "synchronizer")

(2) : Debug mode is working properly only with external DACs via SPI interface. Forced will be kept when in "debug mode".

Debug mode is not working properly when used with internal DAC's. The forced value will be overriden by AFC, AGC or ALC units.

(3): Response has one frame delay added compares to SPI external DAC.

3.13.1 Automatic Frequency Correction

DM 256 provides Automatic Frequency Correction (AFC) to compensate for any discrepancy in oscillator output frequencies between a Subscriber Station and the Base Station. This discrepancy can occur when a Subscriber Station is located in an area where the temperature is different from that of the Base Station.

3.13.2 Automatic Power Control

DM 256 provides Automatic Level Control (ALC) and Automatic Gain Control (AGC) to compensate for the distance separation between each Subscriber Station and the Base Station. Both ALC and AGC are performed at the Subscriber Stations.

3.13.2.1 Automatic Level Control

ALC serves to adjust the transmit power level of the Subscriber Station. At the Base Station, DM 256 determines the receive power level of each data symbol that it receives. This information becomes part of the statistics header that is prepended to the corresponding data symbol when it is added to the Rx payload buffer. This information can be sent inside a MAC PDU to the Subscriber Station which can then write the required transmit power in the ALC register.

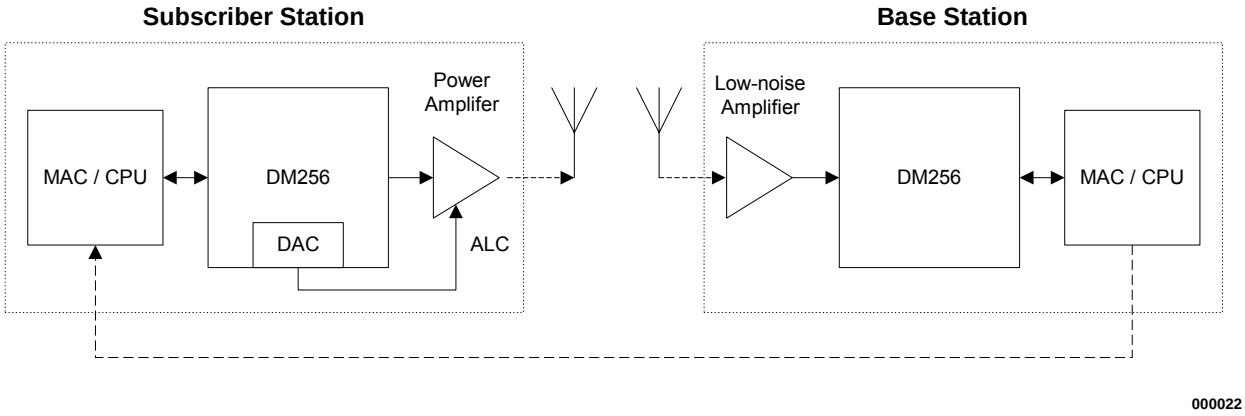


Figure 23: Automatic Level Control

3.13.2.2 Automatic Gain Control

AGC is used by the Subscriber Station to adjust the receive power level. As each Subscriber Station varies in distance from the Base Station, each of them adjusts it's receive power level depending on how far it is from the Base Station.

The AGC analyzes incoming data in a control loop to automatically set the receive gain to the optimum value for demodulation of the OFDM symbols. It also serves to adjust the gain automatically and rapidly in the event of sudden signal level changes.

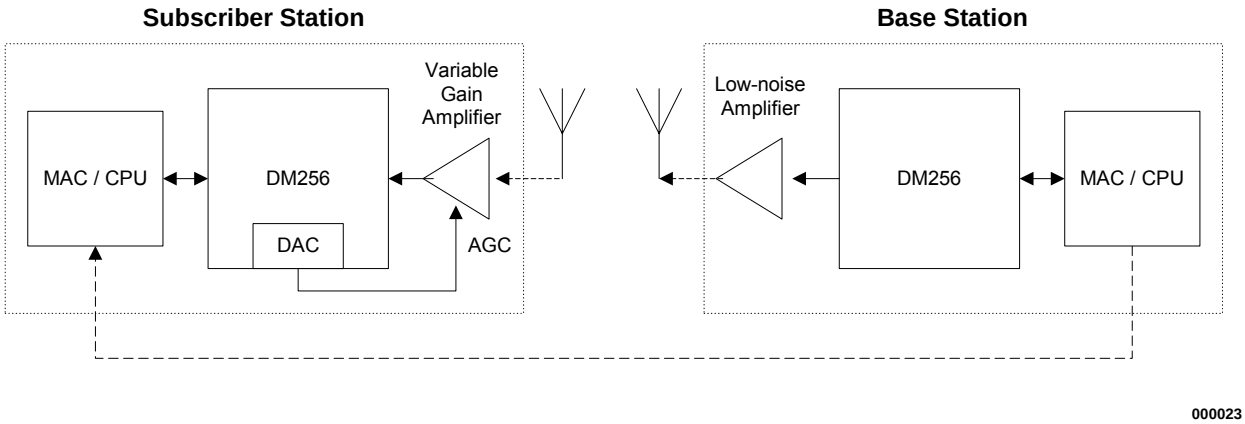


Figure 24: Automatic Gain Control

3.14 Clock Reference Diversity

DM 256 provides a control bit and output that can be used to change the clock reference. This control signal is accessible through a register in the processor interface as a convenience. It drives a signal available to the RF card to select either its own reference clock or an external reference clock if so equipped.

3.15 Antenna Diversity

DM 256 provides a control bit and output that can be used to switch receivers as follows: The MAC Layer sets the control bit to 1 to initiate the process. The antenna switch will usually not occur right away. DM 256 will wait for the end of the current frame before raising the Antenna Select signal.

This signal is synchronized to the end of the receive frame. However, if the signal is bad enough that synchronization is lost or cannot be established, the switch will occur after a period of 22 mS (max). (The 22mS comes from the AGC circuit which has its own timer for the same reason - i.e. when synchronization is not established.)

3.16 MAC Layer Functions

The Mac Layer is responsible for the following functions:

- Determination of the DL and UL frame configuration.
- Negotiating connection by the Subscriber Station, which includes establishment of coding rates, modulation, power levels and transmission delay.
- Scheduling of DL and UL frames for Subscriber Station access, including contention slots for connection attempts by Subscriber Stations.
- Segmentation of messages into MAC PDUs for transmission.
- Re-assembly of received uncoded data blocks into MAC PDUs.
- Fitting MAC PDUs into PHY SDUs.

This page has been left intentionally blank.

Section: 4 Setup and Configurations

4.1 Startup/Reset Mode

Upon startup or reset, DM 256 falls into the Standby/Test mode by default. This mode blocks the incoming data, from the modulator interface, which can cause corruption in the receive path when the feedback modes are changed. During normal transmission, the Tx Enable bit and the Operate Mode bit must be set to enable transmission.

4.2 Setting Up the DM 256

The Wavesat DM 256 OFDM requires some preliminary configuration before normal operation can begin. Some of these configuration options have some design considerations that will be discussed later. The configuration options are listed below:

- Control Register.
- Digital IF Register 1.
- Digital IF Register 2.
- Synchronization Threshold Register.
- Force Synchronization Threshold Register.
- Configuration Value Register.
- PAPR Scaling Register.
- DMA Control Registers.
- CP Size Register.

Table 45: Control Registers

Control Register	Descriptions
Tx Enable	This bit controls the forwarding of data from the PAPR Reduction stage to the Digital IF stage. For normal data transmission, this bit needs to be set to 1.
Tx Base Station Mode	This bit must be set to 1 for Base Stations.
Rx Base Station Mode	This bit must be set to 1 for Base Stations.

4.2.1 Digital IF Register 1

Table 46: Digital IF Register 1

Digital IF Register1	Descriptions
Tx Mute Lead Value	Set this bit to the desired number of samples to advance the enabling of the modulator's PA ahead of the burst.
Tx Mute Lag Value	Set this bit to the desired number of samples to continue the enabling of the modulator's PA after the end of the burst.
Tx Digital IF	Set this bit to the desired modulation output
Rx Digital IF	Set this bit to the desired modulation input.
Tx BW Mode	Set this to the desired channel bandwidth.
Rx BW Mode	Set this to the desired channel bandwidth.

4.2.2 Digital IF Register 2

Table 47: Digital IF Register 2

Digital IF Register 2	Descriptions
Rx Center-to-Sample Frequency Ratio	Set this to the desired value.
Tx Center-to_sample Frequency Ratio	Set this to the desired value.

4.2.3 Synchronization Threshold Register

Table 48: Synchronization Threshold Register

Synchronization Threshold Register	Descriptions
REF1 Auto-Correlation Threshold	This value must be set to 125.
REF2 Auto-Correlation Threshold	This value must be set to 188.
REF1 Cross-Correlation Threshold	This value must be set to 63.

4.2.4 Force Synchronization Threshold Register

Table 49: Force Synchronization Threshold Register

Force Synchronization Threshold Register	Descriptions
Force REF Threshold	This value must be set to 1.

4.2.5 Configuration Value Register

Table 50: Configuration Value Register

Configuration Value Register	Descriptions
Tx Gain Value	This value is an unsigned integer

4.2.6 PAPR Scaling Register

Table 51: PAPR Scaling Registers

PAPR Scaling Register	Descriptions
PAPR Tx Scaling Factor:	This value must be set to -1

4.2.7 DMA Control Registers

Table 52: DMA Control Registers

DMA Control Registers	Descriptions
Rx DMA Transfer Width	This field must be set to the appropriate value if the bus width to the Rx Payload Buffer is not 32 bits
Rx DMA	Set this to 1 if the transfer of Rx Payload is controlled by the DM 256 via DMA.
Tx DMA	Set this to 1 if the transfer of Tx Payload is controlled by the DM 256 via DMA.

4.2.8 CP Size Register

Table 53: CP Size Register

CP Size Register	Descriptions
FCH Rate ID	This value should be set to 6 (BPSK-1/2).
CP Size	This should be set to one of (8, 16, 32, or 64) for CP sizes (1/32, 1/16, 1/8, and ¼) respectively.

4.3 Finding the Correct Cyclic Prefix (CP) Size

For a Subscriber Station to achieve DM 256 synchronization with the Base Station, it must first determine the correct CP size in use. The DM 256's control register is programmed with one of the four valid CP sizes. Then a measurement of the number of FCH symbols received versus the number of Rx Frames received during a fixed interval of time is made. The interval should be sufficiently long to get an accurate estimation.

Considering that the longest frame duration is 20 ms, this would yields 50 frames per second. Therefore something in the order of 0.5 second should yield at least 25 Rx Frames. If the number of FCH symbols received is > ½ the number of frames received, then the DM 256 can be considered synchronized. If not, another CP size is chosen and the process is repeated until synchronization is achieved.

Note:	If the CP size is known by some other means, then it may be programmed directly into the DM 256's control register and this step can be skipped.

4.4 Loopback Testing

DM 256 provides the following loopback for troubleshooting purposes:

Raw data loopback (1).
Packet loopback (2).
Encoded word loopback (3).
Sample feedback (4).

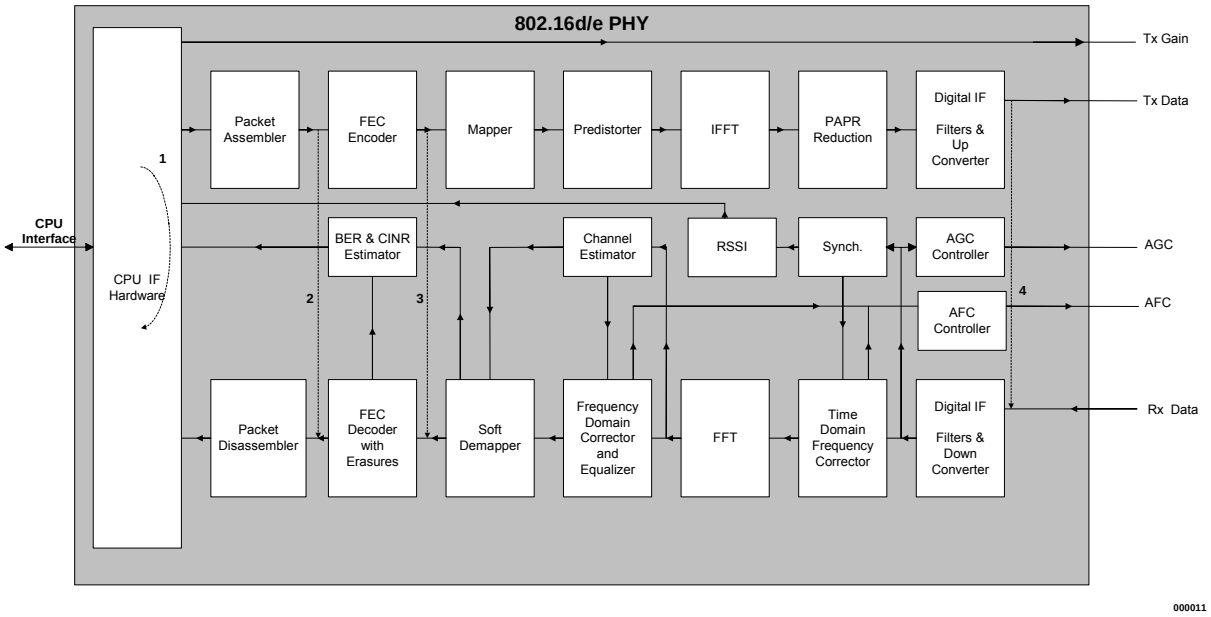


Figure 25: Loopback Testing

Packet loopback (2) and encoded word loopback (3) must have the Standby/Test Mode bit (Bit 17 of the Control Register) set before and during the test. The Test mode blocks the Rx data from being injected into the receive path. This mode must be set for 7 symbol periods to allow any existing data to be flushed out of the receive path. In addition, any previously generated frames must be allowed to end transmission. By waiting for the Tx configuration control bits to clear and then waiting 7 symbol periods, this requirement will be met.

4.5 Serial Port Connections

The two synchronous serial ports on DM 256 can be used to connect Bit Error Rate (BER) test equipment directly to the Tx and Rx payload buffers. The serial ports can also replace the parallel access between the processor and the buffers.

Specifications:

- Simple handshake to validate the data to minimize the use of glue logic.
- Voltage level of 3.3V.
- Tx serial port clock can go up to 50 MHz.
- Rx serial port clocked at 50 MHz (system clock).
- For pin-outs, refer to Table 63: Pin Assignments.

To use the serial ports, DM 256 must be placed in serial mode and the serial ports enabled (bits 26 and 27 of the control register. Table 54: Serial port and mode configuration explains the configuration depending on the settings of the serial mode and serial port.

Table 54: Serial port and mode configuration

Serial mode	Serial port	Configuration
0	0	The serial port is disabled (normal setting). The Tx payload buffer transmits parallel data to the CPU and the Rx payload buffer receives parallel data from the CPU.
0	1	Behavior undefined (do not use this configuration)
1	0	The serial port is emulated. This configuration serves to test the serial port module. In this mode, the payload from the MAC Layer is serialized before it is fed to the Tx serial port modules. In the Rx channel, the data received is also serialized and fed to the Rx serial port modules as if it is coming from the serial port.
1	1	The serial port is enabled. The Tx payload buffer transmits data to the serial port and the Rx payload buffer receives data from the serial port.

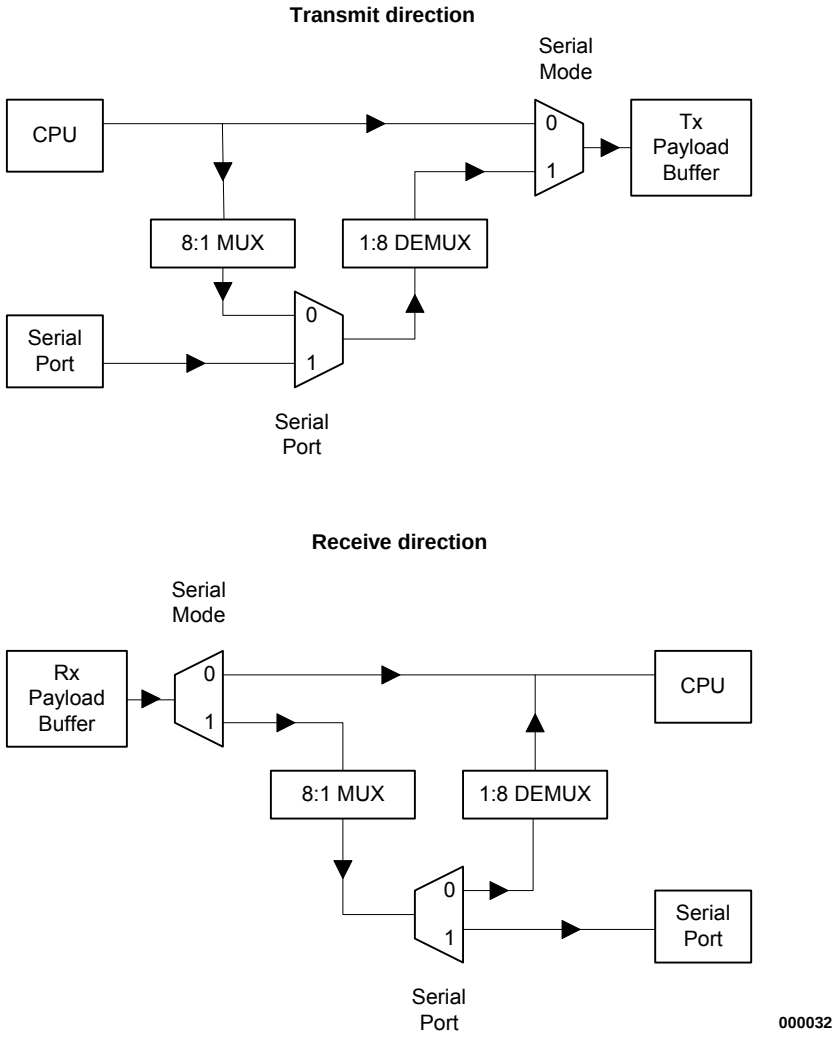


Figure 26: Block diagram of the Serial Port and Mode Configuration

Section: 5 Signal and Pin Descriptions

5.1 Signal Groups

Table 55: Signal Groups

Signal Groups		
Signals	**No. of pins**	**Description**
CPU interface	63	This interface is a generic 32-bit CPU interface.
RF interface	29	This interface connects to the RF transceiver.
ADC/DAC control	21	This interface connects to the RF transceiver.
SPI port	5	This interface can be used to connect to external DACs.
Serial port	9	This interface provides access to and from the data buffers on the host side to provide an alternative method of data input/output to/from the DM 256 controlled channel. Data transmitted over this interface must be raw data or externally formatted. The serial interface supports a maximum of 50 Mbits/sec in each direction (Tx and Rx) non-coded bit rate for future compatibility with the HSAR.
JTAG interface	5	This interface is used for the purpose of boundary scan.
Others	11	
Total	**143**	

5.2 Signal Descriptions

Table 56: CPU Interface Signal Descriptions

CPU Interface				
Signal	**Pin numbers**	**Digital/Analog**	**Direction**	**Description**
Clk	162	Digital	In	System clock 50 MHz
Reset_n	41	Digital	In	Reset (active low)
CS	79	Digital	In	Chip select signal for processor access (active low)
PD [31:0]	Note 1	Digital	In/Out	Processor data bus
PA [15:2]	Note 1	Digital	In	Processor address lines
PRW	84	Digital	In	Processor peripheral bus R/W signal (read=1, write=0)
IRQ [3]	69	Digital	Out	PHY interrupts
DMA_Req [3:0]	71, 72, 73, 78	Digital	Out	DMA request (active high)
DMA_Ack [3:0]	83, 82, 81, 80	Digital	In	DMA acknowledge (active high)
PWE [3:0]	60, 61, 64, 65	Digital	In	Write enable byte (active low)
NOTE 1: See Pin Assignments table (in the following section) for pin numbers.				

Table 57: RF Interface Signal Descriptions

RF Interface				
Signal	**Pin numbers**	**Digital/Analog**	**Direction**	**Description**
Tx_Clk	182	Digital	In	40 MHz clock is provided to the ADC and the DAC for Sampling Clock (for data output).
Rx_Digital_IF [9:0]	Note 1	Digital	In	Digital IF input
Tx_Digital_IF [9:0]	Note 1	Digital	Out	Digital IF output
ADC_Vin_Ip	20	Analog	In	Differential analog positive I input in I/Q mode Differential analog IF input in IF mode
ADC_Vin_In	21	Analog	In	Differential analog negative I input in I/Q mode Differential analog IF input in IF mode
ADC_Vin_Qp	17	Analog	In	Differential analog positive Q input in I/Q mode Not used in IF mode
ADC_Vin_Qn	16	Analog	In	Differential analog negative Q input in I/Q mode Not used in IF mode
DAC_Vout_Ip	2	Analog	Out	Differential analog positive I output in I/Q mode Differential analog positive IF output in IF mode
DAC_Vout_In	1	Analog	Out	Differential analog negative I output in I/Q mode Differential analog negative IF output in IF mode
DAC_Vout_Qp	7	Analog	Out	Differential analog positive Q output in I/Q mode Not used in IF mode
DAC_Vout_Qn	8	Analog	Out	Differential analog negative Q output in I/Q mode Not used in IF mode
NOTE 1: See Pin Assignments table (in the following section) for pin numbers.				

Table 58: ADC/DAC Control Signal Descriptions

ADC/DAC Control				
Signal	**Pin numbers**	**Digital/Analog**	**Direction**	**Description**
ALC	203	Analog	Out	Analog ALC output (Tx Gain)
AGC	202	Analog	Out	Analog AGC output (Rx Gain)
AFC	204	Analog	Out	Analog AFC output
ADC_Ibias	15	Analog	Out	Output for monitoring internal bias current generator
ADC_VCM	22	Analog	Out	Output for monitoring internal common mode voltage
ADC_Vrefp	13	Analog	Out	Output of internal reference voltages
ADC_Vrefn	14	Analog	Out	Output of internal reference voltages
ADC_AVdd	12, 23	Analog	In/Out	ADC analog voltage supply
ADC_AGnd	11, 24	Analog	In/Out	ADC analog ground
DAC_AVdd	4, 5, 206, 207	Analog	In/Out	DAC analog voltage supply
DAC_AGnd	3, 6, 205, 208	Analog	In/Out	DAC analog ground
Vref_In	10	Analog	In	Reference voltage for analog section (input)
Vref_out	9	Analog	Out	Reference voltage for analog section (output)
NOTE 1: See Pin Assignments table (in the following section) for pin numbers.				

Table 59: Serial Peripheral Interface (SPI) Signal Descriptions

Serial peripheral interface (SPI)				
Signal	**Pin numbers**	**Digital/Analog**	**Direction**	**Description**
SPI_CS0	56	Digital	Out	Tx ALC control (Active Low)
SPI_CS1	55	Digital	Out	Rx AGC control (Active Low)
SPI_CS2	54	Digital	Out	Rx AFG control (Active Low)
SPI_Clk	59	Digital	Out	SPI clock
SPI_Data	53	Digital	Out	SPI data
NOTE 1: See Pin Assignments table (in the following section) for pin numbers.				

Table 60: Serial Port Interface Signal Descriptions

Serial Port Interface				
Signal	**Pin numbers**	**Digital/Analog**	**Direction**	**Description**
Serial_Clk_In	177	Digital	In	Tx serial clock input (0 @ 50 MHz)
Serial_Clk_Out	178	Digital	Out	Rx serial clock output (50 MHz)
Serial_Din	181	Digital	In	Tx serial data input
Serial_Dout	175	Digital	Out	Rx serial data output
Serial_Din_Valid_n	176	Digital	In	Tx serial valid signal (active low)
Serial_Dout_Valid_n	172	Digital	Out	Rx serial valid (active low), this signal is asserted when the payload is valid.
Serial_Dout_Valid	173	Digital	Out	Rx serial valid (active high), this signal is asserted when the payload is valid.
Serial_Dout_Start_n	174	Digital	Out	Rx serial start (active low), this signal is asserted when the statistical header is valid
Serial_Ready_n	166	Digital	Out	Rx serial FIFO ready signal (active low)
NOTE 1: See Pin Assignments table (in the following section) for pin numbers.				

Table 61: JTAG Interface Signal Descriptions

JTA Interface				
Signal	**Pin numbers**	**Digital/Analog**	**Direction**	**Description**
JTAG_TMS	153	Digital	In	Test mode select
JTAG_TCK	156	Digital	In	Test clock
JTAG_TDI	155	Digital	In	Test data in
JTAG_TDO	154	Digital	TS0	Test data out
JTAG_TRST_n	152	Digital	In	Test reset (active low)
NOTE 1: See Pin Assignments table (in the following section) for pin numbers.				

Table 62: Other Signal Descriptions

Others			
Signal	**Pin numbers**	**Direction**	**Description**
Antenna_Switch	165	Out	Antenna selection signal synchronized to start of frame
Ext_Ref_En	70	Out	Control RF section for internal or external reference clock
LED_Tx	42	Out	Transmit activity LED (active low)
LED_Rx	43	Out	Receive activity LED (active low)
LED_Pwr_On	44	Out	Power-On LED
GPS_1PPS	161	In	GPS synchronization (one pulse per second)
Tx_Frame_Sync	163	Out	End of Tx frame pulse (pull-down)
BIST_En	159	In	Built-in self-test enable (pull-down) * This signal must be tied to ground.
Scan_En	160	In	Scan enable (pull-down) * This signal must be tied to ground.
Tx_Mute	164	Out	Disable the transmitter (active low)
Gap_Pulse	151	Out	Output to Cheetah for channel switching
NOTE 1: See Pin Assignments table (in the following section) for pin numbers.			

Note:
All signals are active high unless otherwise noted.
All signals are clocked out on the rising edge unless other wise noted.

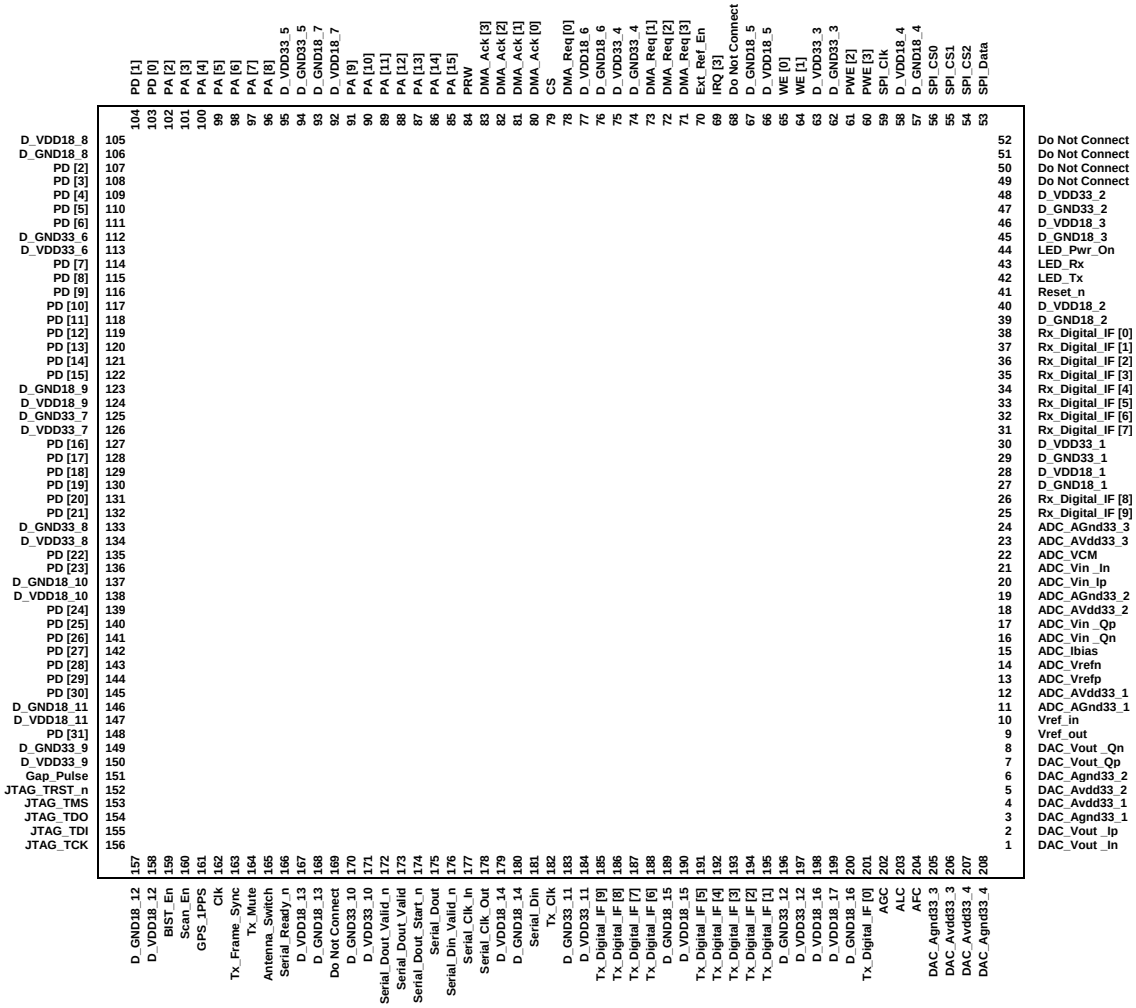
5.3 Pin Assignments

Table 63: Pin Assignments

1	DAC_Vout _In	53	SPI_Data	105	D_VDD18_8	157	D_GND18_12
2	DAC_Vout _Ip	54	SPI_CS2	106	D_GND18_8	158	D_VDD18_12
3	DAC_Agnd33_1	55	SPI_CS1	107	PD [2]	159	BIST_En
4	DAC_Avdd33_1	56	SPI_CS0	108	PD [3]	160	Scan_En
5	DAC_Avdd33_2	57	D_GND18_4	109	PD [4]	161	GPS_1PPS
6	DAC_Agnd33_2	58	D_VDD18_4	110	PD [5]	162	Clk
7	DAC_Vout_Qp	59	SPI_Clk	111	PD [6]	163	Tx_Frame_Sync
8	DAC_Vout _Qn	60	PWE [3]	112	D_GND33_6	164	Tx_Mute
9	Vref_out	61	PWE [2]	113	D_VDD33_6	165	Antenna_Switch
10	Vref_in	62	D_GND33_3	114	PD [7]	166	Serial_Ready_n
11	ADC_AGnd33_1	63	D_VDD33_3	115	PD [8]	167	D_VDD18_13
12	ADC_AVdd33_1	64	WE [1]	116	PD [9]	168	D_GND18_13
13	ADC_Vrefp	65	WE [0]	117	PD [10]	169	Do Not Connect
14	ADC_Vrefn	66	D_VDD18_5	118	PD [11]	170	D_GND33_10
15	ADC_Ibias	67	D_GND18_5	119	PD [12]	171	D_VDD33_10
16	ADC_Vin _Qn	68	Do Not Connect	120	PD [13]	172	Serial_Dout_Valid_n
17	ADC_Vin _Qp	69	IRQ [3]	121	PD [14]	173	Serial_Dout_Valid
18	ADC_AVdd33_2	70	Ext_Ref_En	122	PD [15]	174	Serial_Dout_Start_n
19	ADC_AGnd33_2	71	DMA_Req [3]	123	D_GND18_9	175	Serial_Dout
20	ADC_Vin_Ip	72	DMA_Req [2]	124	D_VDD18_9	176	Serial_Din_Valid_n
21	ADC_Vin _In	73	DMA_Req [1]	125	D_GND33_7	177	Serial_Clk_In
22	ADC_VCM	74	D_GND33_4	126	D_VDD33_7	178	Serial_Clk_Out
23	ADC_AVdd33_3	75	D_VDD33_4	127	PD [16]	179	D_VDD18_14
24	ADC_AGnd33_3	76	D_GND18_6	128	PD [17]	180	D_GND18_14
25	Rx_Digital_IF [9]	77	D_VDD18_6	129	PD [18]	181	Serial_Din
26	Rx_Digital_IF [8]	78	DMA_Req [0]	130	PD [19]	182	Tx_Clk
27	D_GND18_1	79	CS	131	PD [20]	183	D_GND33_11
28	D_VDD18_1	80	DMA_Ack [0]	132	PD [21]	184	D_VDD33_11
29	D_GND33_1	81	DMA_Ack [1]	133	D_GND33_8	185	Tx_Digital_IF [9]
30	D_VDD33_1	82	DMA_Ack [2]	134	D_VDD33_8	186	Tx_Digital_IF [8]
31	Rx_Digital_IF [7]	83	DMA_Ack [3]	135	PD [22]	187	Tx_Digital_IF [7]
32	Rx_Digital_IF [6]	84	PRW	136	PD [23]	188	Tx_Digital_IF [6]
33	Rx_Digital_IF [5]	85	PA [15]	137	D_GND18_10	189	D_GND18_15
34	Rx_Digital_IF [4]	86	PA [14]	138	D_VDD18_10	190	D_VDD18_15
35	Rx_Digital_IF [3]	87	PA [13]	139	PD [24]	191	Tx_Digital_IF [5]
36	Rx_Digital_IF [2]	88	PA [12]	140	PD [25]	192	Tx_Digital_IF [4]
37	Rx_Digital_IF [1]	89	PA [11]	141	PD [26]	193	Tx_Digital_IF [3]
38	Rx_Digital_IF [0]	90	PA [10]	142	PD [27]	194	Tx_Digital_IF [2]
39	D_GND18_2	91	PA [9]	143	PD [28]	195	Tx_Digital_IF [1]
40	D_VDD18_2	92	D_VDD18_7	144	PD [29]	196	D_GND33_12
41	Reset_n	93	D_GND18_7	145	PD [30]	197	D_VDD33_12
42	LED_Tx	94	D_GND33_5	146	D_GND18_11	198	D_VDD18_16
43	LED_Rx	95	D_VDD33_5	147	D_VDD18_11	199	D_VDD18_17
44	LED_Pwr_On	96	PA [8]	148	PD [31]	200	D_GND18_16
45	D_GND18_3	97	PA [7]	149	D_GND33_9	201	Tx_Digital_IF [0]
46	D_VDD18_3	98	PA [6]	150	D_VDD33_9	202	AGC
47	D_GND33_2	99	PA [5]	151	Gap_Pulse	203	ALC
48	D_VDD33_2	100	PA [4]	152	JTAG_TRST_n	204	AFC
49	Do Not Connect	101	PA [3]	153	JTAG_TMS	205	DAC_Agnd33_3
50	Do Not Connect	102	PA [2]	154	JTAG_TDO	206	DAC_Avdd33_3
51	Do Not Connect	103	PD [0]	155	JTAG_TDI	207	DAC_Avdd33_4
52	Do Not Connect	104	PD [1]	156	JTAG_TCK	208	DAC_Agnd33_4

000038

5.4 Pin Assignment Diagram



00038

Figure 27: Pin Assignment Diagram

5.5 DAC Connection Diagram

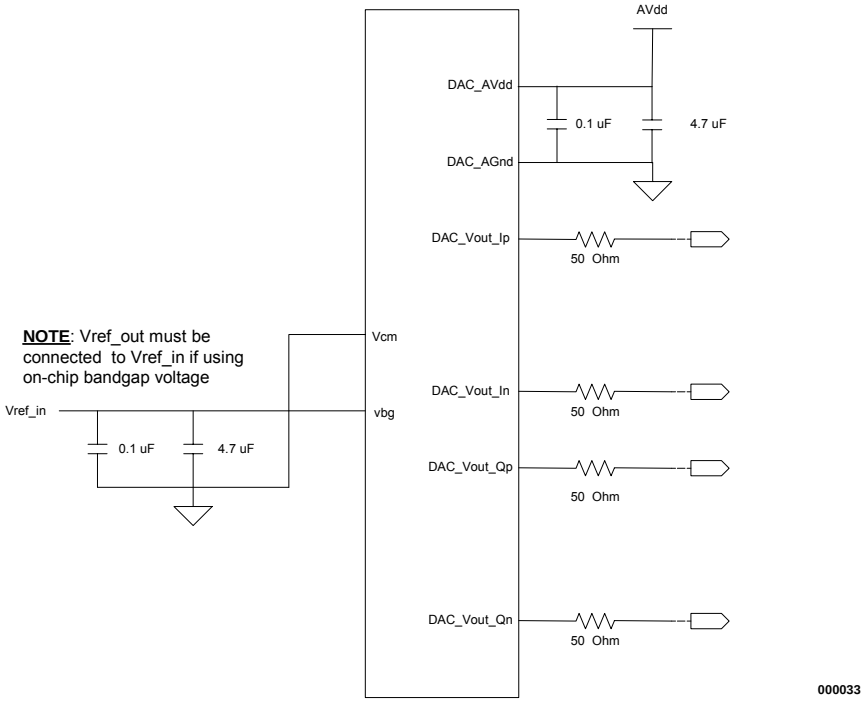


Figure 28: DAC Connection Diagram

5.6 ADC Connection Diagram

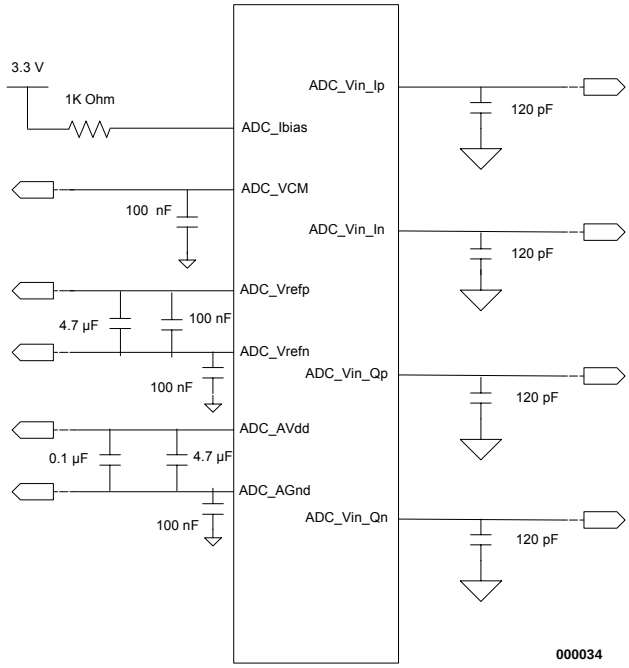


Figure 29: ADC Connection Diagram

5.7 Reference Voltage Distribution for DM256

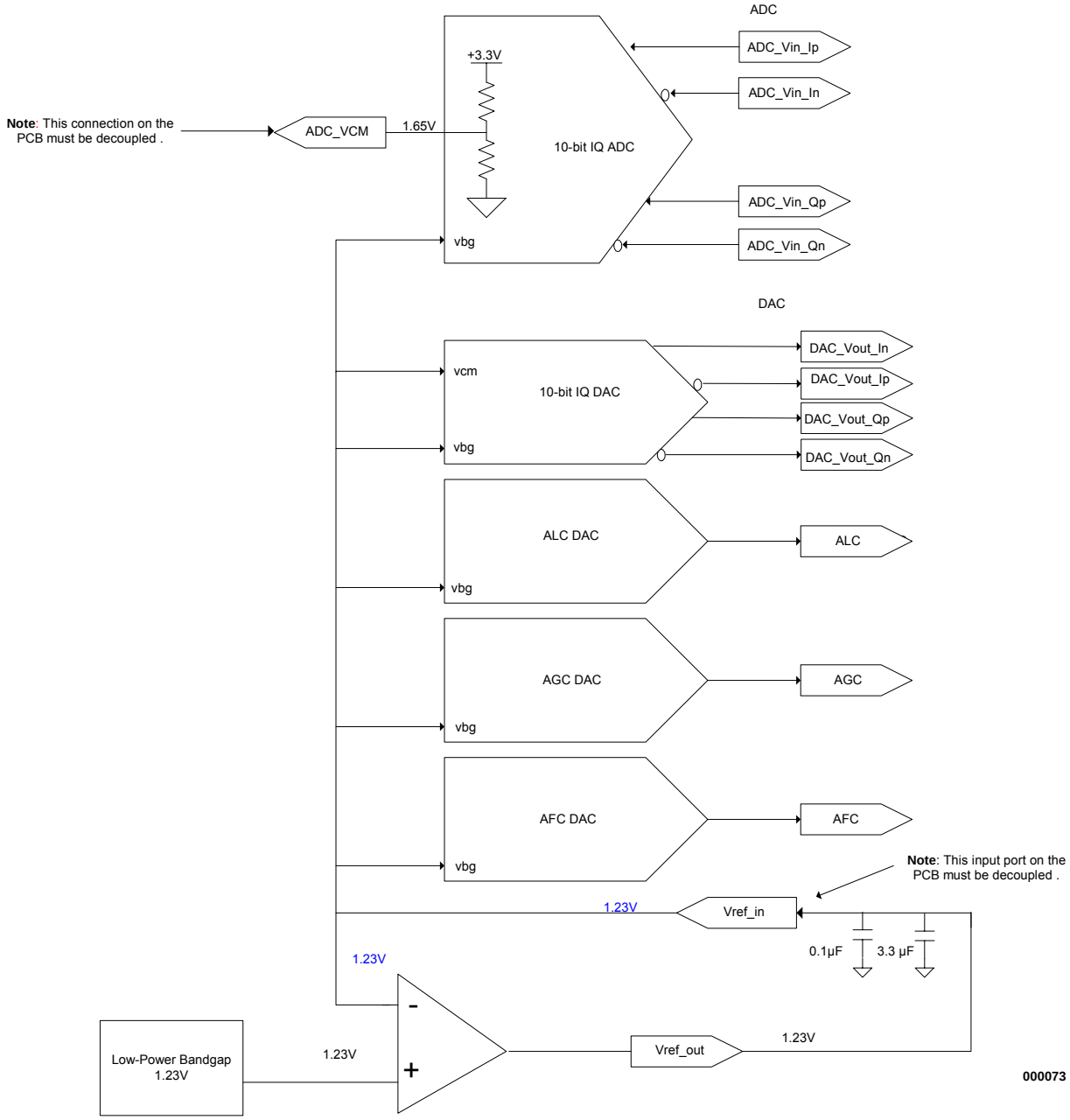


Figure 30: Reference Voltage Distribution Diagram

Section: 6 Register Descriptions

6.1 Endianness Convention

DM 256 uses a bus and register bit naming convention where the number 0 represents the Least Significant Bit (LSB) and the number 31 represents the Most Significant Bit (MSB) in Big-Endian Notation.

6.2 Register Address Table

Table 64: Register Address Table

Address	Mode	Description	Base Station typical setting	Subscriber Station typical setting
0000	R	Status Register	0x00000B0B	0x00000B0B
0004	R/W	Control Register	0x73020001	0xA0020001
0008	R	Revision Control Register	0x57020042	0x57020042
000C	R/W	Interrupt Control/Status Register	0x000001FD	0x000001FD
0010	R/W	DMA Control Register 1	0xF0000000	0xF0000000
0014	R/W	Frame Configuration Buffer Control Register	0x0000000A	0x00000011
0018	R/W	Base ID Register	0x00000000	0x00000000
001C	R/W	Force Synchronization Register (factory test only)	0x00000004	0x00000004
0020	R/W	Synchronization Threshold Register (factory test only)	0x047E0000	0x05780000
0024	R/W	Delay Correction (Ranging) Register	0x00000000	0x00000413
0028	R	Lost-Packet Count Register	0x00000000	0x00000000
002C	R	Frame Number Register	0x00020FB0	0x0002329E
0030	R/W	Force Configuration Register	0x00000004	0x00000004
0034	R/W	Configuration Value Register	0x0000000A	0x0000000A
0038	R/W	DMA Control Register 2	0x42264000	0x40004000
003C	R/W	PDU Filter Control Register	0x00000000	0x00000000
0040	R	PDU Filter Lost Packet Control Register	0x00000000	0x00000000
0044	R/W	Digital IF Register 1	0x00000220	0x00000220
0048	R/W	Digital IF Register 2	0x1ADF1ADF	0x1ADF1ADF
004C	R/W	Peak-to-Average Power Ratio (PAPR) Control Register	0x00000000	0x00000000
0050	R/W	Tx Mute Control Register	0x0000043C	0x0000043C
0054	R/W	Cyclic Prefix (CP) Size Register	0x00000010	0x00000010
0058	R/W	SPI Interface Register	0xD0020703	0xD0020703
005C	R/W	DAC Register 1	0x00000600	0x00510600
0060	R/W	DAC Register 2	0x00002001	0x20012001
0064	R/W	Analog Control Register	0x088C0003	0x0B8C0003
0068	R/W	Analog Value Register	0x20080000	0x20080000
006C	R	SNR and Average Power Register	0x00020000	0x00050000
1000 - 1FFF	R/W	Tx/Rx Payload Buffers (This address is used by the Tx payload buffer on write and by the Rx payload buffer on read.)		
2000 - 2FFB	R/W	Tx Frame Configuration Buffer 1		
2FFC - 3FF7	R/W	Tx Frame Configuration Buffer 2		
4000 - 4FFB	R/W	Rx Frame Configuration Buffer 1		
4FFC - 5FF7	R/W	Rx Frame Configuration Buffer 2		
NOTE: For more details on each register, see the following subsections.				

6.3 Status Register

This register provides information on the state of the receive link. It also indicates the received power level (measured over the preamble).

Table 65: Status Register

Bit	Mode	Name	Description
0	R	Rx Link Active	1 = At least one preamble detected in the last two frames 0 = No preamble not detected in the last two frames
1	R	Rx Link Configured	1 = FCH detected in incoming frame 0 = FCH not detected in incoming frame
2	R	Rx Data Ready	1 = Rx data buffer is ready to transmit data to the MAC Layer. This occurs when the buffer is up to ¾ of its capacity.
3	R	Tx Data Ready	1 = Tx data buffer is ready to receive data from the MAC Layer. This occurs when the buffer is down to ¼ of its capacity.
31-4		Not used	

6.4 Control Register

The control register serves for enabling and disabling various functions of the DM 256.

Table 66: Control Register

Bit	Mode	Name	Description
0	R/W	Tx Channel Enable	1 = Normal setting 0 = Transmission is unconditionally muted. (Data are discarded at the Digital IF stage.)
1	R/W	Bad-Data Filter On	1 = Data uncorrected by the Reed–Solomon Convolutional Coding (RS-CC) are discarded. 0 = Normal setting (All data are passed through and sent to the Rx Payload buffer.)
2	R/W	Tx Randomizer Off	1 = The randomizer is unconditionally disabled. 0 = Normal setting
3	R/W	Tx Convolutional Encoder Off	1 = The Convolutional (inner) Encoder is unconditionally disabled. 0 = Normal setting
4	R/W	Tx RS Encoder Off	1 = The Reed-Solomon (outer) Encoder is unconditionally disabled. 0 = Normal setting
5	R/W	Tx Interleave Off	1 = The Interleaver is unconditionally disabled. 0 = Normal setting
6	R/W	Tx Payload Buffer Reset	1 = The contents of the Tx payload buffer is cleared. 0 = Normal setting
7	R/W	Rx Noise Inducer On	1 = Enables an internal noise generator for Factory testing. 0 = Normal setting

8	R/W	Tx PRBS On	1 = Pseudo Random Bit Sequence (PRBS) is generated in lieu of stuffing bits. 0 = Normal setting
9	R/W	Rx Frequency Offset Correction Off	1 = The frequency compensation algorithm is disabled. 0 = Normal setting
10	R/W	Rx Phase Offset Correction Off	1 = The phase correction algorithm is disabled. 0 = Normal setting
11	R/W	Rx Payload Buffer Reset	1 = The contents of the Rx payload buffer is cleared. 0 = Normal setting
12	R/W	Rx De-randomizer Off	1 = The de-Randomizer is unconditionally disabled. 0 = Normal setting
13	R/W	Rx De-interleaver Off	1 = The de-Interleaver is unconditionally disabled. 0 = Normal setting
14	R/W	Rx RS Decoder Off	1 = The Reed-Solomon (outer) Decoder is unconditionally disabled. 0 = Normal setting
15	R/W	PDU pass-through On	1 = All symbols are sent to the Rx payload buffer. 0 = Normal setting (Only data symbols are sent to the Rx payload buffer.)
16	R/W	Rx Convolutional Decoder Off	1 = The Convolutional (inner) decoder is unconditionally disabled. 0 = Normal setting
17	R/W	Operate Mode	1 = Normal setting 0 = Standby/test mode Upon reset, DM 256 starts in standby mode and blocks incoming data from the modulator interface. To enable normal operation, the host must initialize all registers to normal settings before setting this bit.
18	R/W	GPS Slave On	1 = Base station slave mode 0 = Normal setting If the DM 256 is configured to be base station in transmission, slave mode will allow the DM 256 to synchronize DL frames to a GPS 1 pulse per second synchronization signal. This function requires that the 40 TX sample clock by phase locked to the GPS as well.
19	R/W	Reserved	Must be set to 0
20	R/W	Data Feedback On	1 = Internal self-diagnostic test (Raw data written to the Tx payload buffer are looped back to the Rx payload buffer. In this mode, the Tx channel mode must be set to 1 and the Rx channel mode set to 0.) 0 = Normal setting
21	R/W	Packet Feedback On	1 = Internal self-diagnostic test (Data written to the Tx payload buffer are looped back at the packet assembling and segmenting stages. In this mode, the Tx channel mode must be set to 1 and the Rx channel mode set to 0. 0 = Normal setting
22	R/W	Encoded Word Feedback On	1 = Internal self-diagnostic test (Data written to the Tx payload buffer are looped back at the encoding and decoding stages. In this mode, the Tx channel mode must be set to 1 and the Rx channel mode set to 0.) 0 = Normal setting

23	R/W	Sample Feedback On	1 = internal self-diagnostic test (Data written to the Tx payload buffer are looped back at the IF conversion stages. All input digital IF signals are blocked.) 0 = Normal setting
24	R/W	Tx Channel Mode	1 = DM 256 operates in Base Station Mode for transmission. 0 = DM 256 operates in Subscriber Station Mode for transmission.
25	R/W	Rx Channel Mode	1 = DM 256 operates in Base Station mode for reception. 0 = DM 256 operates in Subscriber Station mode for reception.
26	R/W	Serial Mode	1 = Set to 1 to use the serial port if serial port is enabled or to emulate the serial port if the serial port is disabled 0 = Set to 0 when the serial port is disabled. Do not set to 0 if the serial port is enabled.
27	R/W	Serial Port	1 = The serial port is enabled. The Tx payload buffer transmits data to the serial port and the Rx payload buffer receives data from the serial port. The Serial Mode must be set to 1. 0 = Normal setting. The serial port is disabled. The Tx payload buffer transmits data to the host and the Rx payload buffer receives data from the host. The Serial Mode must be set to 0 during normal operation and can be set to 1 to emulate the serial port.
31-28	R/W	Test Port	Test signal select (for Factory testing only)

6.5 Revision Control Register

This register provides identification and release information on the DM 256 chip.

Table 67: Revision Control Register

Bit	Mode	Name	Description
7-0	R	Build	
15-8	R	Revision number	
23-16	R	Software version	01 = FPGA load 02 = ASIC load
31-24	R	Company identification	87

6.6 Interrupt Control and Status Register

This register is used by the host to generate an interrupt on several events. To enable the interrupt on each of these events, the host must set the corresponding bit to 1 in write mode. When one of these events occurs, DM 256 generates an interrupt and sets the corresponding bit to 1 in read mode. The interrupt request line is tri-stated when no interrupt source is enabled. The interrupt is automatically cleared once the bit is read.

Table 68: Interrupt Control and Status Register

Bit	Mode	Name	Description
0	R/W	Rx data ready	1 = Rx data buffer is ready to transmit data to the MAC Layer. This occurs when the buffer is ≥ to ¾ of its capacity. When the buffer is < ¾ of its capacity, then the Rx data ready is disabled if the serial port is enabled.
1	R/W	Tx data ready	1 = Tx data buffer is ready to receive data from the MAC Layer. This occurs when the buffer is ≤ to ¼ of its capacity.
2	R/W	Start of REF2	1 = indicates the start of a frame at the Subscriber Station and at the Base Station it indicates the reception of a REF2 symbol
3	R/W	Rx Payload Buffer overflow	1 = The Rx payload buffer has overflowed. (Any incoming data are discarded.)
4	R/W	End of Tx Frame	1 = indicates the end of a Tx frame. The Tx Frame IRQ interrupt is generated when the last sample of the frame has clocked out.
5	R/W	FCH symbol received	1 = Indicates that an FCH burst has been detected. This bit applies only to Subscriber Stations.
6	R/W	Tx Payload Buffer Reset	1 = The Tx payload buffer is reset due to either of the following conditions: 1) Mismatch between the Tx frame data and the Tx frame configuration. 2) Late frame request; i.e. the Subscriber Station receives a request to burst in an earlier frame with respect to the frame number register.
7	R/W	Internal header error	1 = The DM 256 has encountered an unrecoverable error.
8	R/W	Frame Configuration Error	1 = An invalid value has been detected in the frame configuration data. (For example, the FFT size can only be 256. Therefore if any other value is entered in its field, the Frame Configuration Error will be generated).
9	R/W	Tx Payload Buffer Underrun	1 = Indicates that there was a transmission underrun and the DM 256 inserted one or more 0xFF stuffing bytes.
31-10		Not used	

6.7 DMA Control Register 1 and 2

Two registers are used for DMA control.

DMA Control Register 1 permits DM 256 to generate DMA transfer requests for the following:

Tx payload buffer.
Rx payload buffer.

The following table lists the channels.

Table 69: DMA Control Register 1

DMA Control Register 1			
Bit	**Mode**	**Name**	**Description**
29-0		Not used	
30	R/W	Rx Payload DMA Enable	1 = Enable DMA request for Rx payload. Request will be temporarily halted on full transmit buffer.
31	R/W	Tx Payload DMA Enable	1 = Enable DMA request for Tx payload. Request will be temporarily halted on empty receive buffer.

DMA Control Register 2 sets the DMA transfer width. It also provides a count of bytes contained in the Tx payload buffer and in the Rx payload buffer. These counts can be queried regardless of whether the DMA is enabled or not.

Table 70: DMA Control Register 2

DMA Control Register 2			
Bit	**Mode**	**Name**	**Description**
12-0	R	Rx Payload Count	Receive buffer content (number of bytes in buffer)
13		Not used	
15-14	R/W	Rx DMA Transfer Width	00 =: Word (default) 01 = Byte 10 = Half word 11 = Word
28-16	R	Tx Payload Count	Transmit buffer content (number of bytes in buffer)
31-29		Not used	

6.8 Frame Configuration Buffer Control and Status Register

This register controls when to read from the frame configuration buffers and when to write to them.

Table 71: Frame Configuration Buffer Control and Status Register

Bit	Mode	Name	Description
0	R/W	Tx Configuration Buffer 1 Ready	The MAC Layer sets this bit when the buffer is ready to be read by the DM 256. When set, the bit queues the construction and the transmission of the bursts in the corresponding Frame Configuration Buffer. The bit is automatically cleared to 0 by the DM 256 after the frame has been transmitted and the alternate Tx Frame Configuration Buffer is set to 1. When the bit is cleared, the MAC Layer can write to the Tx Frame Configuration Buffer and set the bit to 1 again.
1	R/W	Tx Configuration Buffer 2 Ready	The MAC Layer sets this bit when the buffer is ready to be read by the DM 256. When set, the bit queues the construction and the transmission of the bursts in the corresponding Frame Configuration Buffer. The bit is automatically cleared to 0 by the DM 256 after the frame has been transmitted and the alternate Tx Frame Configuration Buffer is set to 1. When the bit is cleared, the MAC Layer can write to the Tx Frame Configuration Buffer and set the bit to 1 again.
2		Not used	Not used
3	R/W	Rx Configuration Buffer 1 Ready	The MAC Layer sets this bit when the buffer is ready to be read by the DM 256. When set, the bit queues the demodulation and the decoding of bursts in the corresponding Frame Configuration Buffer. The bit is automatically cleared to 0 by the DM 256 after the frame has been received and the alternate Rx Frame Configuration Buffer is set to 1. When the bit is cleared, the MAC Layer can write to the Rx Frame Configuration Buffer and set the bit to 1 again.
4	R/W	Rx Configuration Buffer 2 Ready	The MAC Layer sets this bit when the buffer is ready to be read by the DM 256. When set, the bit queues the demodulation and the decoding of bursts in the corresponding Frame Configuration Buffer. The bit is automatically cleared to 0 by the DM 256 after the frame has been received and the alternate Rx Frame Configuration Buffer is set to 1. When the bit is cleared, the MAC Layer can write to the Rx Frame Configuration Buffer and set the bit to 1 again.
31-5		Not used	Not used

6.9 Base Station Identification Register

This register controls when the DM 256 does not decode burst in the DLFP for which the BSID Field does not match.

Table 72: Base Station Identification Register

Bit	Mode	Name	Description
3-0	R/W	BSID	The 4 Least Significant Bits of the Base Station ID
4	R/W	BSID Enable	When this bit is set to 1, the DM 256 does not decode bursts in the DLFP for which the BSID Field does not match.
31-5		Not used	

6.10 Force Synchronization Register

This register controls when the DM 256 uses the Reference Threshold in the Synchronization Threshold Register.

Table 73: Force Synchronization Register

Bit	Mode	Name	Description
1-0		Not used	
2	R/W	Force Reference Threshold	When set to 1, this bit forces the DM 256 to use the Reference Threshold in the Synchronization Threshold Register
31-3		Not used	

6.11 Synchronization Threshold Register

This register controls the sensitivity of the synchronizer for reference recognization.

Table 74: Synchronization Threshold Register

Bit	Mode	Name	Description
7-0		Not used	
15-8	R/W	REF1 Auto-Correlation Threshold	This value must be set to 125.
23-16	R/W	REF2 Auto-Correlation Threshold	This value must be set to 188.
31-24	R/W	REF2 Cross-Correlation Threshold	This value must be set to 63.

6.12 Ranging Offset Register

This register is used to store the Ranging Offset value obtained during ranging to compensate for the delay in which the Base Station receives a burst from each Subscriber Station. This register is used at the Subscriber Stations only.

Initial ranging is performed as follows: At power-up, the Subscriber Station detects and synchronizes with the long preamble transmitted by the Base Station. The Subscriber Station can then extract the ULMAP to determine the Initial Ranging Interval. The Substation then transmits a Ranging Request (RNG-REQ) message to the Base Station in the Initial Ranging Interval. Based on the delay in which the Base Station receives the message, it returns a Ranging Response (RNG-RSP) message indicating the correction value to apply to this register. The Subscriber Station uses the correction value to advance or delay its transmission such that Subscriber Station will appear to be co-located with the Base Station.

Table 75: Ranging Offset Register

Bit	Mode	Name	Description
15-0	R/W	Ranging Offset	16 bit unsigned number of sample periods to advance or delay transmission.
31-16		Not used	

6.13 Lost-Packet Count Register

This register is used only if the Bad-Packet Filter (register address 0004, bit 2) is enabled.

Table 76: Lost Packet Count Register

Bit	Mode	Name	Description
15-0	R	Number of discarded packets	Indicates the number of packets that have been discarded due to uncorrectable errors in the Reed–Solomon decoding since the power-up or reset
31-16		Not used	

6.14 Frame Number Register

At the Subscriber Station, DM 256 increments the frame number each time it detects the long preamble f the incoming frame. This information is used to ensure the frame payload, identified by the frame number register, matches the frame configuration data.

At the Base Station, the DM 256 increments this register each time a frame is transmitted.

Table 77: Frame Number Register

Bit	Mode	Name	Description
23-0	R	Rx frame number	Indicates the frame number of the current frame.
31-24		Not used	

6.15 Force Configuration Register

A digital gain factor can be applied to the Tx and/or Rx signals when the appropriate bit in this register is set to '1'. The digital gain factor is stored in the Configuration Value Register.

Table 78: Force Configuration Register

Bit	Mode	Name	Description
1-0		Not used	
2	R/W	Force Tx gain	1 = Force Tx gain specified in the Configuration Value Register
3	R/W	Force Rx gain	1 = Force Rx gain specified in the Configuration Value Register
31-4		Not used	

6.16 Configuration Value Register

A digital gain factor can be applied to the Tx and/or Rx signals and is stored in this register. The gain factor is applied only when the appropriate bit in the Force Configuration Register is set to 1.

Table 79: Configuration Value Register

Bit	Mode	Name	Description
7-0	R/W	Tx gain value	Unsigned integer (0-255)
31-8		Not used	

6.17 Digital IF Register 1 and 2

Digital IF Register 1 contains control bits and bandwidth selection values.

Table 80: Digital IF Register 1

Bit	Mode	Name	Description
0	R/W	Force Tx bandwidth and center frequency	1 = Force Tx digital IF to use selected bandwidth and center frequency When '1', TX bandwidth and TX "center freq" (digital IF Register 2), must be set. 0 = Use default values (bandwidth: 3.5 MHz; center frequency: 1/4 of sample clock)
1	R/W	Force Rx bandwidth and center frequency	1 = Force Rx digital IF to use selected bandwidth and center frequency When '1', RX bandwidth and RX "center freq" (digital IF Register 2), must be set. 0 = Use default values (bandwidth: 3.5 MHz; center frequency: 1/4 of sample clock)
2	R/W	Rx Digital IF Input	1 = Complex numbers (IQ inputs used). **Must be = 1 when Bit 15 = 1.** Allow complex input when IF or I/Q mode. 0 = Real numbers
3	R/W	Tx Continuous Mode	1 = Output is a single carrier frequency (sine wave) at a frequency set in "Digital IF Register2" for RF debugging. (Continuous wave mode) 0 = Normal operating mode.
7-4	R/W	Tx bandwidth selection	0001 = 1.75 MHz 0010 = 3.5 MHz 0011 = 7 MHz 1001 = 10 MHz
11-8	R/W	Rx bandwidth selection	0001 = 1.75 MHz 0010 = 3.5 MHz 0011 = 7 MHz 1001 = 10 MHz
12	R/W	Tx DAC Digital Bus Mode	Mode 1 = 2's Complement (Mode 1 for default built in DAC's) Mode 0 = Straight Bit Format.
13	R/W	Rx ADC Digital Bus Mode	Mode 1 = 2's Complement (Mode 1 for default built in ADC's) Mode 0 = Straight Bit Format.
14	R/W	Tx Digital IF Output	1 = Complex numbers (IQ Format) . For IQ baseband, you must set the TX "center freq" to "0". For IF complex, simply set a tx "center freq" at the desired frequency when IQ format is selected. 0 = IF mode format (Real Values Only)
15	R/W	Rx Digital IF Input	1 = IQ baseband Format. You must set the RX "center freq" to "0" when IQ is selected. **If set to1 then Bit 2 = 1 (complex input)** 0 = IF mode format (Real or Complex values depending on Bit 2 setting (1=Real, 0=Complex)).
31-16		Not used	

The bit configuration for each channel bandwidth selection is as follows:

The Digital IF Register 2 is divided into two 16-bit fields, each of which is used to set the center frequency in the transmit or receive direction.

Table 81: Digital IF Register 2

Bit	Mode	Name	Description
15-0	R/W	Tx Center Frequency	See following equation NOTE: You must set the “center freq” to “0” when TX Digital IF IQ baseband format is required (Digital IF Register 1, bit 14).
31-16	R/W	Rx Center Frequency	See following equation NOTE: You must set the “center freq” to “0” when RX Digital IF IQ baseband format is required (Digital IF Register 1, bit 15).

The center frequency is set by entering a ratio, which is the Desired Center Frequency (Hz) to the Sample Clock Frequency (Hz) right shifted by 16 bits

$$x = \left(\frac{DesiredCenterFreq}{(SampleClockFreq / 2^{16})} \right)$$

and is rounded to the nearest multiple of 16.

$$Center\_to\_Sample\_CLK\_Ratio = 16 * floor[x/16]$$

For example, given a 40 MHz sample clock frequency and a desired Transmit Center Frequency of 3.5 MHz, the resulting ratio is 5728.

Note:	There is no limitation on the value specified for the Desired Center Frequency for either the Tx or the Rx registers. For example, if the Desired Center Frequency for the Tx is specified to be –5000000 Hz, then an inverted image of the signal will be transmitted with a center frequency of 5 Mhz.

Note:	For the analog output, there is no analog filtering of the images created by the digital to analog conversion

Note:	There is a predistorter in the chip designed to compensate for the sin(x)/x effect for the lowest frequency image, i.e. the predistorter compensates for the effect when the IF of the image is within [0, Fs/2].

The following figures illustrate some of the possible ways to configure the I/Q-low IF interface.

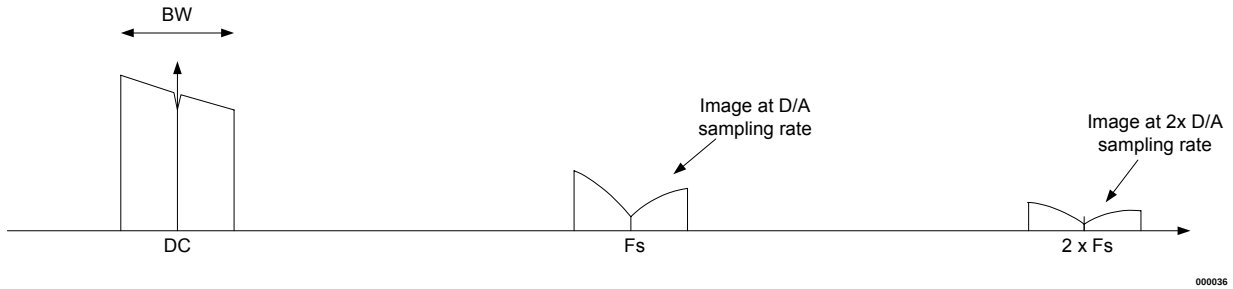


Figure 31: I/Q baseband, analog output

Figure 32: Low IF (IF frequency = BW/2), I/Q analog output

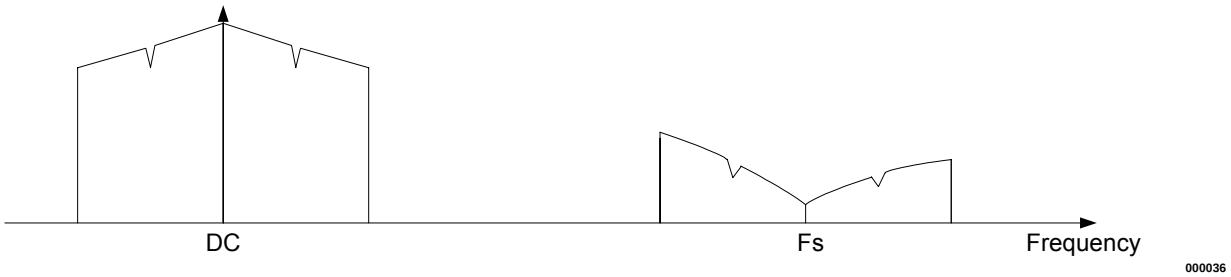


Figure 33: Low IF (IF frequency = BW/2), real-valued analog output

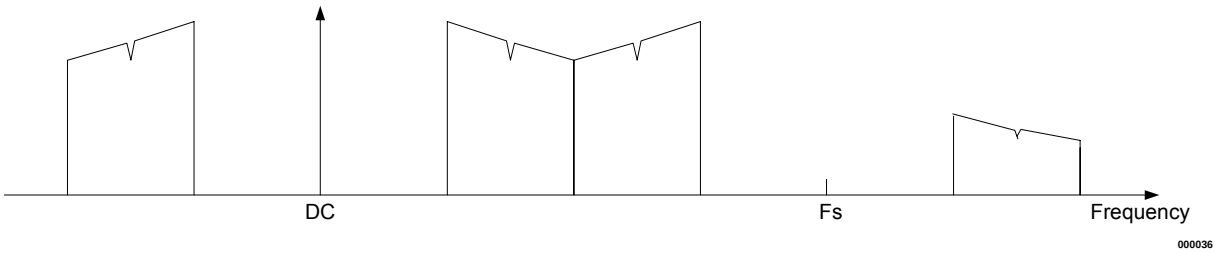


Figure 34: Low IF (IF frequency = Fs – BW/2), real-valued analog output

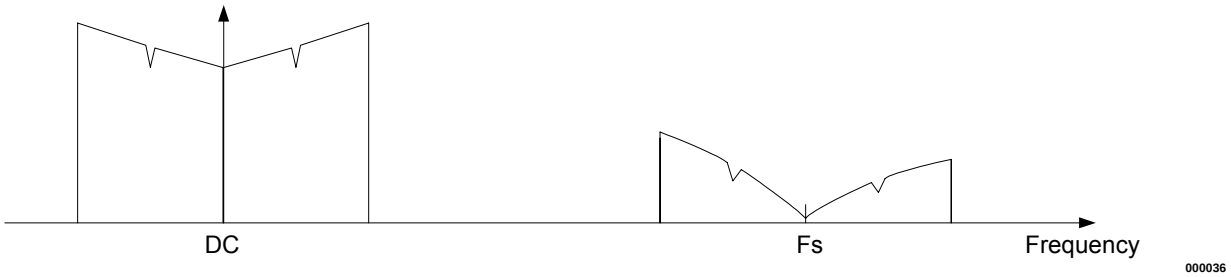


Figure 35: Low IF (IF frequency = – BW/2), real-valued analog output

6.18 Peak-to-Average Power Ratio (PAPR) Control Register

This register applies a scaling factor to improve the Peak-to-Average Power performance by scaling the output of the FFT (Fast Fourier Transform).

The PAPR of the transmission can be controlled by the combination of two settings:

A PAPR register is used to set the amount of bit shifting applied to the time domain samples.
A Tx gain register is used to set the amount of gain, from 0 to 1 applied to the frequency domain samples.

Table 82: Peak to Average Power Ratio Control Register

Bit	Mode	Name	Description
3-0	R/W	PAPR Tx scaling factor value	Signed number A positive value increases the FFT scaling, thus decreasing the output level. A negative value decreases the FFT scaling, thus increasing the output level. However, when increasing the output, saturation of the sample values will occur. The amount of saturation is traded off with the increase in output level. Empirically, -1 has been found to be the optimal value with a default TX gain (255)
7-4	R/W	PAPR Rx scaling factor value	Signed number RX scaling factor works the same as TX except that it is the resultant frequency domain samples that are scaled. Normally, this scaling factor is kept at 0
31-8		Not used	

6.19 Tx Mute Control Register

This register is used to control the TXMUTE signal. This function is required in TDD and HFDD systems where the transmitter must be muted during the receive stage. In FDD systems, the transmitter is always operating and using a frequency different than that of the receiver.

Table 83: Tx Mute Control Register

Bit	Mode	Name	Description
7-0	R/W	Tx mute lead value	Unsigned integer. This setting is used in Auto Tx Mute to advance the transmitter mute for the specified duration before the last sample is clocked out of the Tx payload buffer. Normal setting is 60.
15-8	R/W	Tx mute lag value	Unsigned integer. This setting is used in Auto Tx Mute to delay the transmitter mute for the specified duration after the last sample is clocked out of the Tx payload buffer. Normal setting is 4.
16	R/W	External Synchronization Reference Enable	1: Indicates that an external clock is being used 0: Indicates that the internal clock is being used
17	R/W	Antenna Switch Enable	This bit allows you to switch between two transceivers.
18	R/W	Auto Tx Mute Disable	1: Disable auto Tx mute 0: Enable auto Tx mute
19	R/W	Tx Mute Enable (manual switch)	1 = Set Tx mute 0 = Remove Tx mute
31-20		Not used	Not used

6.20 Cyclic Prefix (CP) Size Register

This register sets the Cyclic Prefix (CP) size and the modulation rate used for the Frame Control Header (FCH).

Table 84: Cyclic Prefix Size Register

Bit	Mode	Name	Description
7-0	R/W	CP Size (in samples)	64 samples = ¼ 32 samples = 1/8 16 samples = 1/16 08 samples = 1/32 For example, to enter a CP size of 1/32, enter 08. The default CP size is 0.
11-8	R/W	FCH Rate ID	0 = QPSK ½ 1 = QPSK ¾ 2 = 16-QAM ½ 3 = 16-QAM ¾ 4 = 64-QAM 2/3 5 = 64-QAM ¾
31-12		Not used	

6.21 SPI Interface Register

DM 256 uses an SPI interface to control external digital-analog converters (DAC) via the Serial Peripheral Interface (SPI). These DACs are used to control the ALC (Tx gain), AGC (Rx gain), and AFC in normal closed-loop application. The SPI Interface register is used to test and debug the devices attached on the SPI bus, thus bypassing the normal control algorithms.

Table 85: SPI Interface Register

Bit	Mode	Name	Description
0	R/W	SPI Interface Enable	0 = Disabled 1 = Enabled
1	R/W	SPI Manual Mode	The ALC (Tx gain), AGC (Rx gain), and AFC are normally automatically adjusted by DM 256 based on feedback via the statistical header. However, when the Manual Mode is enabled, these DACs are set using data in bits 16-31. 0 = Disabled 1 = Enabled
2	R/W	Force SPI Clock	0 = Disabled 1 = Enabled
3		Not used	
7-4	R/W	SPI Clock Speed	0 = 6.250 MHz 1 = 3.125 MHz 2 = 1.562 MHz 3 = 781.250 kHz 4 = 390.625 kHz 5 = 195.312 kHz 6 = 97.656 kHz 7 = 48.828 kHz 8 = 24.414 kHz 9 = 12.207 kHz 10 = 15: 6.250 MHz
8	R/W	ALC DAC Select	0 = Disabled 1 = Enabled
9	R/W	AGC DAC Select	0 = Disabled 1 = Enabled
10	R/W	AFC DAC Select	0 = Disabled 1 = Enabled
15-11		Not used	
31-16	R/W	SPI Data	The 8-bit value written in bits 16-31 are applied to the selected DAC when SPI Manual Mode is set to 1. Only one DAC can be selected at a time.

6.22 DAC Register 1

DAC Register 1 is used by the Subscriber Stations, Base Stations and by each station to adjust its Automatic Level Control (ALC) or output level, respectively. When the Base Station receives a burst from a Subscriber Station, it measures the power level at which the burst was received. This information becomes part of the header that is prepended to each MACPDU and transmitted to the MAC Layer. Power adjustment messages can be transmitted back to the Subscriber Station inside a MAC PDU to update the ALC register. The content of the ALC register is used to adjust the transmit amplifier power at the Subscriber Station

Table 86: DAC Register 1

Bit	Mode	Name	Description
9-0	R/W	ALC value	ALC value (Unsigned integer) Set value directly to the ALC DAC
10	R/W	ALC enable	1 = ALC enable, enables the ALC module 0 = Default setting
15-11		Not used	
23-16	R/W	VGA value	Is a set contact valued for the AGC algorithm in the AGC Module The variable gain amplifier (VGA) value is a factor that is combined with AGC value to set the receive gain. The VGA value must be determined by the user based on the type of amplifier used and entered to the register as follows. The reciprocal of the VGA gain is calculated and then converted to a binary representation using a 12-bit resolution. The result is then entered to the register. For example, the receive amplifier used by Wavesat has a VGA gain of 50. The VGA gain reciprocal is 1/50 = .02. Converting .02 to a binary value using a 12-bit resolution = 000001010001. B(000001010001) = D(81)
31-24		Not used	

6.23 DAC Register 2

DAC Register 2 is used by each Subscriber Stations only and is used by each station for the following:

Automatic Frequency Correction (AFC)
Automatic Gain Control (AGC)

The AFC is used by each Subscriber Station to compensate for the discrepancy in oscillator output frequency between the Subscriber Station and the Base Station. The discrepancy can be caused by the differences in local environmental condition, such as temperature variation, that can exist between the two stations.

The AGC is required by each Subscriber Station to adjust its receive power level. The Base Station always transmits at the same power. As Subscriber Stations can vary in distance from the Base Station, each Subscriber Station adjusts its receive power level depending on environmental conditions or how far it is from the Base Station. The power level is calculated for every symbol.

Table 87: DAC Register 2

Bit	Mode	Name	Description
0	R/W	AFC enable	1 = AFC enable, this enables the AFC module 0 = Default setting
3-1		Not used	
13-4	R/W	AFC value	AFC value (Unsigned integer) (read-only) Reads value sent to the AFC DAC.
15--14		Not used	
16	R/W	AGC enable	1 = AGC enable, this enables the AGC module 0 = Default setting
19-17		Not used	
29-20	R/W	AGC value	AGC value (Unsigned integer) (read-only) Reads value sent to the AGC DAC.
31-30		Not used	

6.24 Analog Control Register

Table 88: Analog Control Register

Bit	Mode	Name	Description
1-0	R/W	ADC Mode	Digital mode = 0, Rx input are read from 10-bit RX_SAMPLES_PIN bus, Power Down ADC Analog mode = 1, Internal ADC Standby Analog mode = 2, Internal ADC using unsigned binary coding Analog mode = 3, Internal ADC using 2's complement coding
8-2		Not used	For internal Wavesat use only.
15-9		Not used	
16	R/W	Tx DAC input Enable_N	0 = Disabled – Normal Operating Mode. Tx samples DAC values comes from TX digital IF. AFC DAC value comes from AFC module AGC DAC value comes from AGC module ALC DAC value comes from ALC register in the bus interface **For Internal Wavesat Use Only** 1 = Enabled tx samples DAC values comes from Analog value register in the bus interface. AFC DAC value comes from Analog value register in the bus interface. AGC DAC value comes from Analog value register in the bus interface. ALC DAC value comes from Analog value register in the bus interface.
17	R/W	Analog Test I\O Mux Control	0 = Disabled 1 = Enabled
18	R/W	Analog Tx DAC Inphase	0 = Disabled 1 = Enabled
19	R/W	Analog Tx DAC Quadrature	0 = Disabled 1 = Enabled
20		Analog Tx DAC Iref	**For Internal Wavesat Use Only**
21		Analog Tx DAC VCM	**For Internal Wavesat Use Only**
22	R/W	Analog Tx DAC Sleep	0 = Disabled 1 = Enabled
23	R/W	Analog AFC DAC	0 = Disabled 1 = Enabled
24	R/W	Analog AGC DAC	0 = Disabled 1 = Enabled
25	R/W	Analog ALC DAC	0 = Disabled 1 = Enabled
26	R/W	Analog Test Pulse	0 = Disabled, do not latch the values. **For Internal Wavesat Use Only** 1 = Enabled, Latch Analog value from the Analog value register in the bus interface into AFC, AGC and ALC DAC.
27	R/W	Analog Tx Samples	0 = Disabled, the 10-bits digital tx samples pins are driven by the Tx Digital IF 1 = Enabled, t the 10-bits digital tx samples pins are driven to '0'
31-28		Not used	

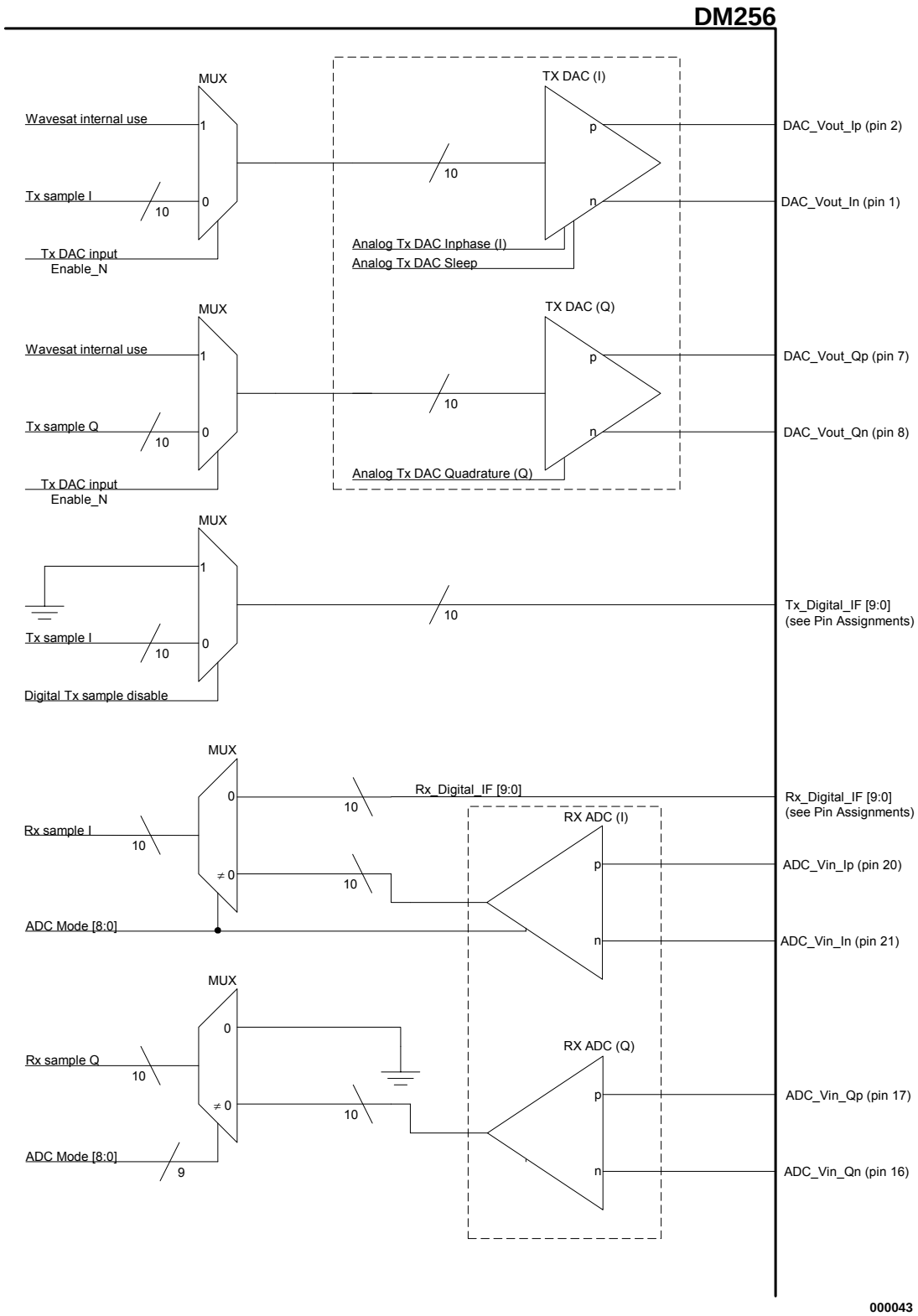


Figure 36: Internal DAC and ADC Control

6.25 Analog Value Register

Note: This is for Test Purposes Only.

Table 89: Analog Value Register

Bit	Mode	Name	Description
9-0	R/W	DAC	Analog DAC value (unsigned integer) Set value for all DACs when in analog test mode. Disable, analog test: tx sample DAC come from Tx Digitial IF, AFC DAC=AFC module, AGC DAC=AGC module, ALC DAC = ALC in the bus interface or Enabled, analog test: tx samples DAC, AFC DAC, AGC DAC, ALC DAC values all come from the Analog register in the bus interface or disable.
19-10	R	ADC In-Phase	Read only – analog ADC in-phase value (unsigned integer) It reads the values obtained by the in phase ADC.
29-20	R	ADC Quadrature	Read only – analog ADC quadrature value (unsigned integer) It reads the values obtained by the quadrature ADC.
31-30		Not used	

6.26 SNR Power Register

Note: This is for Test Purposes Only.

Table 90: SNR Power Register

Bit	Mode	Name	Description
7-0	R	SNR	Read only - Unsigned vector indicating received SNR in dB
15-8	R	Average Power	Read only - Unsigned vector indicating received average power in dB
19-16	R	Symbol Type	Read only - See statistical header section. These values are obtained from the first symbol after a REF1 symbol in a burst i.e. a FCH in DownLink or a data symbol in UpLink.
31-20		Not used	

6.27 Tx/Rx Payload Buffers

Two 4K FIFO buffers are used to store the payload. The MAC Layer writes outgoing payload to the Tx payload buffer for transmission over the air and reads incoming payload from the Rx payload buffer. Both buffers share the same address.

6.28 Tx/Rx Frame Configuration Buffers

DM 256 provides four buffers of 4092 bytes each. They are used by the MAC Layer to write the Frame Desciptors that specify how to modulate the outgoing bursts and demodulate the incoming bursts. The four buffers are:

- Tx Frame Configuration Buffer 1.
- Tx Frame Configuration Buffer 2.
- Rx Frame Configuration Buffer 1.
- Rx Frame Configuration Buffer 2.

Section: 7 Timing, AC Characteristics and Specifications

7.1 Clock Signal Timing

Table 91: Clock Signal Timing

Parameter	Symbol	Min	Typical	Max	Units
CLK input Cycle Time	CK_CYCLE	20	20	TBD	ns
CLK input High/Low Time	CK_HI CK_LO	TBD	TBD	TBD	ns
CLK input Rise/Fall Time	CK_EDGE	0	-	4	ns
Tx_CLK input Cycle Time [1]	DCK_CYCLE	25	25	25	ns
Tx_CLK input High/Low Time	DCK_ HI CK_LO	TBD	TBD	TBD	ns
Tx_CLK input Rise/Fall Time	DCK_ EDGE	0	-	4	ns
TCK input Cycle Time	TCK _CYCLE	100	100	dc	ns
TCK input High/Low Time	TCK _HI CK_LO	40	-	dc	ns
TCK input Rise/Fall Time	TCK _EDGE	0	-	4	ns

7.2 Input/Output Timing

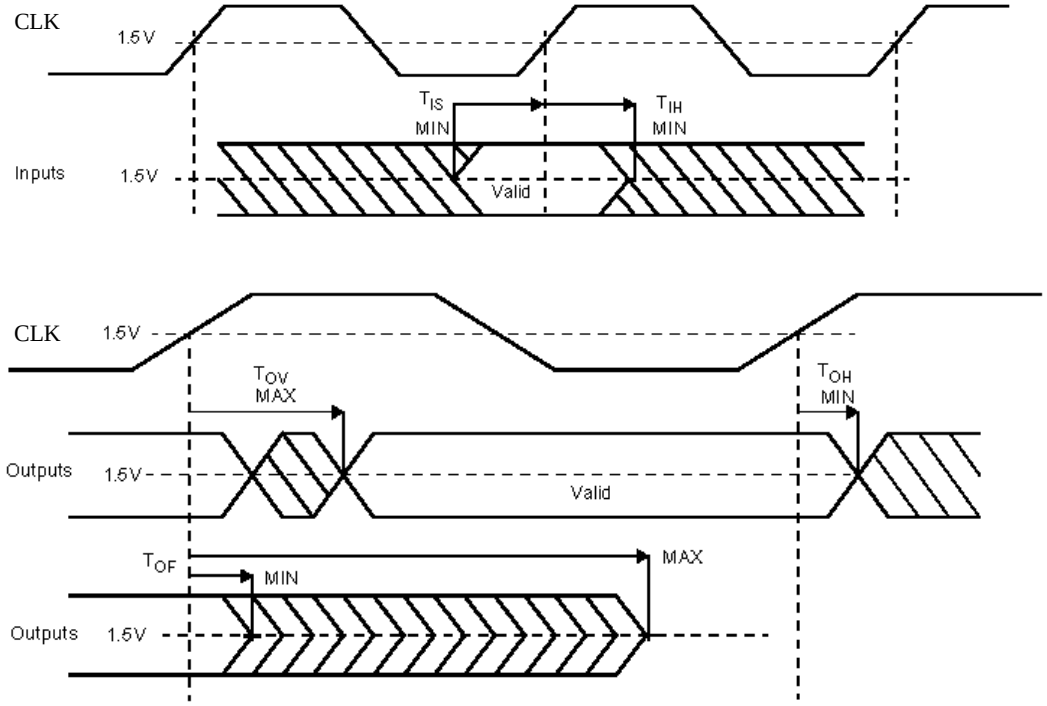


Figure 37: Input/Output Timing Diagram

Table 92: Input/Output Timing

Signals	Inputs (ns)		Outputs (ns)		Clock	Notes
	Setup time (T_{IS} min)	Hold time (T_{IH} min)	Valid delay (T_{OV} max)	Hold time (T_{OH} min)		
RESET, PLL_BP	N/A	N/A				async.
CS, DMA_ACK(3:0), PLLOUT_DIS	8.6	0			CLK	
PA(13:2)	6.6	0			CLK	
PRW	8.6	0			CLK	
DIN(9:0)			20	0	Tx_CLK	
PD(31 =0)	6.6	0	7.6	0	CLK	
IRQ, PLL_OUT, TEST(53:0), DMA_REQ(3:0), CLK_TEST			10	0	CLK	
DOUT(9:0)	30	0			Tx_CLK	
RXMUTE, TXMUTE, LED_Rx, LED_Tx			30	0	CLK	
TDI, TMS, TRST	10	1			TCK	
TDO			10	0	TCK	

7.3 CPU Read and Write Timing

The following diagram shows an example with the PPC405GP processor as the host CPU.

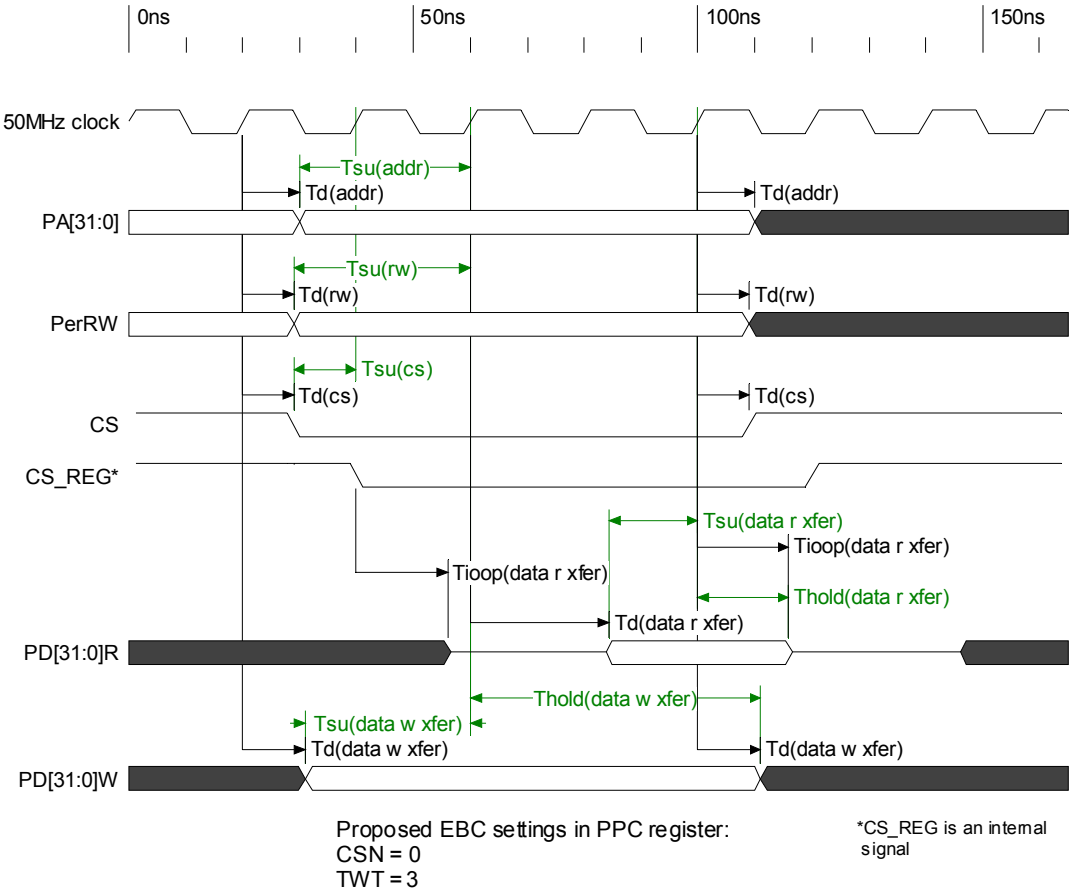
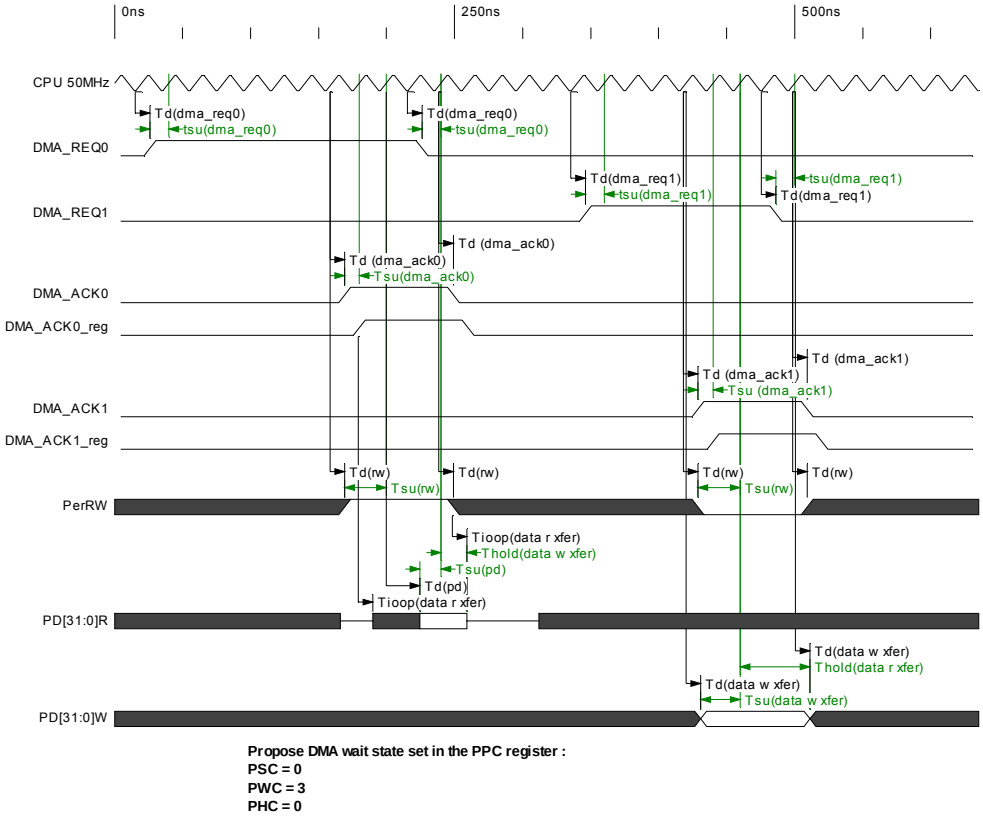


Figure 38: CPU Reading and Writing Timing Diagram

Table 93: CPU Read and Write Timing

Name	Type	Min (ns)	Max (ns)	Description
Td(cs)	Delay		9	Delay time (PerCS)
Td(rw)	Delay		9	Delay time (PerRW)
Tsu(rw)	Constraint	17.94		Setup time (PerRW)
Td(addr)	Delay		10	Delay time (addr)
Tsu(addr)	Constraint	21.49		Setup time (PerAddr)
Td(data w xfer)	Delay		11	Delay time (data write xfer)
Thold(data w xfer)	Constraint	1		Hold time (data write xfer)
Tsu(data r xfer)	Constraint	7		Setup time (data read xfer)
Td(data r xfer)	Delay	24.42		Delay time (data read xfer)
Tioop(data r xfer)	Delay		16	Propagation time (data read xfer)
Thold(data r xfer)	Constraint	1		Hold time (data read xfer)
Tsu(data w xfer)	Constraint	13.38		Setup time (data write xfer)
Tsu(cs)	Constraint	6		

7.4 DMA Read and Write Timing



000031

Figure 39: DMA Reading and Write Timing Diagram

Table 94: DMA Reading and Write Timing

Name	Type	Min (ns)	Max (ns)	Description
Td(dma_rx)	Delay		6	Propagation time (data read xfer)
Td(dma_tx)	Delay		6	Propagation time (data read xfer)
tsu(dma_rx)	Constraint	11.7		Setup time (DMA Tx)
tsu(dma_tx)	Constraint	11.7		Setup time (DMA Rx)
Td (dma_rx)	Delay		9	Propagation time (data read xfer)
Tsu(dma_rx)	Constraint	8.15		Setup time (DMA Rx)
Td (dma_tx)	Delay		9	Propagation time (data read xfer)
Tsu (dma_tx)	Constraint	8.15		Setup time (DMA Tx)
Td(rw)	Delay		9	Propagation time (PerRW)
Tsu(rw)	Constraint	17.94		Setup time (PerRW)
Td(data w xfer)	Delay		11	Propagation time (data write xfer)
Tsu(data w xfer)	Constraint	13.38		Setup time (data write xfer)
Thold(data w xfer)	Constraint	1		Hold time (data write xfer)
Tioop(data r xfer)	Delay		10	Propagation time to Hi-Z
Thold(data r xfer)	Constraint	1		Hold time (data read xfer)
Td(pd)	Delay		24.42	Propagation time (data read xfer)
Tsu(pd)	Constraint	7		Setup time (data read xfer)

7.5 JTAG Port Timing

Table 95: JTAG Port Timing

Parameter	Minimum	Maximum
t_{clk} cycle time	200 ns	n/a
TDI setup to t_{clk} rise time	25 ns	n/a
TMS setup to t_{clk} rise time	25 ns	n/a
TRST setup to t_{clk} rise time	25 ns	n/a
TDI hold time from t_{clk} rise	10 ns	n/a
TMS hold time from t_{clk} rise	10 ns	n/a
TRST hold time from t_{clk} rise	10 ns	n/a
t_{clk} fall to TDO valid	n/a	35 ns
NOTE: These values are based on JTAG limitations.		

This page has been left intentionally blank.

Section: 8 Electrical Characteristics

8.1 Absolute Maximum Ratings

Table 96: Absolute Maximum Rating

Symbol	Description		Units
VDD_{core}	Digital Core voltage (1.8 V) relative to GND	-0.5 to 2.0	V
$VDD_{I/O}$	Digital I/O voltage (3.3V) relative to GND	-0.5 to 4.0	V
AVDD	Analog voltage (3.3V) relative to GND	-0.5 to 4.0	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C
T_J	Junction temperature Plastic packages	+160	°C
NOTE 1: Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time can affect device reliability. **NOTE 2**: Power supplies can turn on in any order.			

8.2 Recommended Operating Conditions

Table 97: Recommended Operating Conditions

Symbol	Description	Min	Max	Units
VDD_{core}	Digital Core voltage (1.8 V) relative to GND , T_J = 0 °C to +85°C	3.3 - 5%	3.3 + 5%	V
$VDD_{I/O}$	Digital I/O voltage (3.3V) relative to GND , T_J = 0 °C to +85°C	3.3 - 5%	3.3 + 5%	V
AVDD	Analog voltage (3.3V) relative to GND , T_J = 0 °C to +85°C	3.3 - 5%	3.3 + 5%	V
T_{IN}	Input signal transition time		250	ns

8.3 DC Characteristics over Recommended Operating Conditions

Table 98: DC Characteristics over Recommended Operating Conditions

Symbol	Description	Min	Max	Units
I_{core}	Digital Core current supply		280	mA
$I_{I/O}$	Digital I/O current supply		29	mA
I_A	Analog current supply		91	mA
I_{Total}	Total current supply		500	mA
I_L	Input or output leakage current	-10	+10	µA
C_{IN}	Input capacitance		8	pF

8.4 DC Input and Output Levels

Table 99: DC Input and Output Levels

Pins	VIL		VIH		VOL	VOH	IOL	IOH
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
CLK RESET CS PA (2 - 15) PRW DMA_REQ (3:0) DIN (0 - 9) DTXCLK JTAG_TMS JTAG_TDI JTAG_TCK JTAG_TRST	-0.5	0.8	2.0	3.6				
PD (0 - 31)	-0.5	0.8	2.0	3.6	0.4	3.0	4	4
IRQ 3 DOUT (0 - 9) JTAG_TDO					0.4	3.0	4	4
TXMUTE					0.4	3.0	4	4
LED_Rx LED_Tx LED_FPGA					0.4	3.0	4	4

NOTE 1: Values for VIL and VIH are recommended input voltages.

NOTE 2: Values for IOL and IOH are guaranteed over the recommended operating conditions at the VOL and VOH test points.

NOTE 3: Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

8.5 Digital and Analog Decoupling Recommendations

8.5.1 Digital Power Decoupling

It is recommended that the system designer place at least one decoupling capacitor pair at each power and ground pin. It is also recommended that these decoupling capacitors receive their power from separate power planes in the PCB, utilizing short traces to minimize inductance. These capacitors should have a value of 0.1 µF. Ceramic SMT (Surface Mount Technology) capacitors should be used to minimize lead inductance, oriented such that connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the power and ground planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (Equivalent Series Resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors- 100 to 330 µF (AVX TPS tantalum or Sanyo OSCON).

8.5.2 Analog Power Supplies

Note that, although the analog and digital supply pins can be connected together, for maximum noise immunity it is recommended that they are kept separated. Furthermore, blocking capacitors should be used in order to obtain the best dynamic characteristics. These capacitors should have a value of 0.1 µF and 3.3 µF.

8.5.3 Vref_in decoupling

As for the power supplies, the Vref_in voltage should be decoupled. These capacitors should have a value of 0.1 µF and 3.3 µF.

8.5.4 Output signals for DAC

All the differential circuit should be routed using the same length and aspect in every possible place, to maximize the symmetry of the circuit.

8.5.5 Input Signals for ADC

All the differential circuit should be routed using the same length and aspect in every possible place, to maximize the symmetry of the circuit. Small 100pF capacitors should be place between each input pin and analog ground at board level. The distance between these capacitors ground connection should be as small as possible.

8.5.6 Reference Voltages for ADC

The reference voltages Vrefp, Vrefn and Vcm must be decoupled externally with large capacitors:

- 2.2µF//100nF between Vrefp and Vrefn;
- 100nF from Vrefp to analog ground, 100nF from Vrefn to analog ground;
- 100nF between Vcm and analog ground.

8.5.7 ADC_IREF for ADC

For testability purpose the ADC_IREF pin should be connected to a 3.3V positive power supply through an external resistor. Current is evaluated by measuring the voltage across the resistor.

8.5.8 Low Power Bandgap

Table 100: Voltage Reference Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Output voltage		1.21	1.23	1.26	V
Startup time	after Vdd is in specs			200	µS
Temperature coefficient	-40 ºC < T < 125 ºC			50	ppm/ºC
Line regulation	2.7V < Vdd < 3.6V			1.5	µV/V
Pssr	DC to 100 Hz	40			dB
	10 kHz to 100 kHz	5			dB
	DC to 100 Hz, Cload = 10pF	40			dB
	10 kHz to 100 kHz, Cload = 10pF	10			dB
Note: Temperature Range : [-40ºC to +85ºC], worst cases of Vdd & Process unless otherwise noted					

8.5.9 Static DAC Electrical Specifications

Table 101: Static DAC Electrical Specifications

Parameter	MIN	TYP	MAX	UNITS
Resolution		10		Bit
Update rate			1	MHz
Analog Output				
Full Scale Output Range Note 1	0		2*vref	
Full Power Bandwidth (loaded by 10kΩ // 22pF)	50			kHz
Settling time within 1 lsb for 785 mV output step			1	ms
Output load	1			kΩ
			100	pF
Power Supply Requirements				
avdd Supply Voltage	3	3.3	3.6	V
vdd! Supply Voltage	1.6	1.8 or 3.3	3.6	V
Total Power Dissipation in active mode		1.6	2.3	mW
Total Power Dissipation in Power Down (including vref)		-	10	mW
Power Up Time Note 1			5	ms
Analog Biasing Requirements				
Reference Voltage (vref)	1	1.25	1.5	V
Input current			1	nA
Dynamic Conversion Characteristics				
Differential Nonlinearity (DNL)	-1	+/- 0.5	1	LSB
Integral Nonlinearity (INL)	-2	+/- 1	2	LSB
Effective number of Bits (ENOB) (50 kHz output signal, 1 MHz update rate, loaded by 10kΩ // 22pF)	8			
Gain + Offset errors (loaded by 10kΩ // 22pF)	-2	+/- 1	2	% vref
Timing Characteristics				
Data setup time before clk falling edge - tdst	25			ns
Data hold time after clk falling edge - tdhld	10			ns
Note 1: The output voltage, referred to gnd, is vout = + 2*vref x data/1024				

8.5.10 10 Bits IQ DAC Electrical Specifications

Table 102: 10 bits IQ DAC Electrical Specifications

Parameter	Conditions	MIN	TYP	MAX	Unit
DC SPECIFICATIONS (Ta=25ºC, *avdd*=3.3V, *dvdd*=1.8V, differential output signal)					
ANALOG OUTPUTS					
Resolution			10		bits
Minimum Load resistance	each single-ended output to Vcm	10			KΩ
Load capacitance	each single-ended output			4	pF
Common Mode Voltage - Vcm		0.9	1.25	1.4	V
Offset error		-2		2	%FS
Gain error		-5		5	%FS
Gain matching		-1		1	%FS
SWITCHING PERFORMANCE					
Data Latency	(Ts=1/Fs)		1	2	Ts
Temperature Coefficients					
Offset Drift		-100		100	ppm of FS/ ºC
Gain Drift		-100		100	ppm of FS/ ºC
Reference Voltage Drift			T.B.D.		
Power Supply					
Analog Supply voltage	*avdd*	3	3.3	3.6	V
Digital Supply voltage	*dvdd*	1.62	1.8	1.98	V
Current Consumption	*Normal Operation @ 3.3V*		22		mA
	Stand-by mode		<1		mA
	Power-down		<1		µA
AC SPECIFICATIONS (Ta=25ºC, *avdd*=3.3V, *dvdd*=1.8V)					
Dynamic Performance					
Update rate	Higher rate possible, see Note 1	44			MSPS
Bandwidth of the output buffer Note 2	-3dB	39	53		MHz
Output noise	Fout < 9.9 MHz		0.5		µV/sqrt(Hz)
Wake Up time	Sleep to On to first conversion time		2		µs
Power On Time	Pwr Dwn to On to first conversion time		6		µs
AC Linearity					
Spurious Free Dynamic Range (SFDR)	Analog Output @ -18dBFS; Fout= 1 MHz		68		dBc
	Analog Output @ 0dBFS Fclk=40MHz; Fout= 9.9 MHz				dBc
Total Harmonic Distortion (T.H.D.)	Fclk=40MHz; Fout= 9.9 MHz; 1V pp		56		dBc
Channel Isolation		58	60		dBc
Note 1: The DAC can be operated up an update rate of 44MSPS, if an 8-bit performance level is accepted. Note 2: For full power bandwidth calculation, please see below.					

8.5.11 10 Bits IQ ADC Electrical Specifications

Table 103: 10 bits IQ ADC Electrical Specifications Part 1

Absolute Maximum Ratings					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Analog Supply Voltage		3	3.3	3.6	V
Bandgap Voltage			1.25		V
Junction Temperature		-40	25	125	°C
Power Supply Ripple		-50		50	mV
Power Supply Slew		-25		25	mV/ns
DC SPECIFICATIONS (Ta=25ºC, avdd=3.3V, dvdd=1.8V, differential output signal)					
ANALOG OUTPUTS					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Resolution			10		bits
Output voltage compliance range Note 1			2		Vppdif
Minimum Load resistance	each single-ended output to Vcm	10			KΩ
Load capacitance	each single-ended output			4	pF
Common Mode Voltage - Vcm		0.9	1.25	1.4	V
Offset error		-2		2	%FS
Gain error		-5		5	%FS
Gain matching		-1		1	%FS
SWITCHING PERFORMANCE					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Data Latency	(Ts=1/Fs)		1	2	Ts
TEMPERATURE COEFFICIENTS					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
Offset Drift		-100		100	ppm of FS/°C
Gain Drift		-100		100	ppm of FS/°C
Reference Voltage Drift			T.B.D.		
Note 1: Output voltage compliance range is defined as the single ended voltage range where the outputs behave as current sources, regardless of the external termination scheme.					

Table 104: 10 bits IQ ADC Electrical Specifications Part 1

AC SPECIFICATIONS (Ta=25ºC, avdd=3.3V, dvdd=1.8V)

DYNAMIC PERFORMANCE

Parameter	Conditions	Min	Typ	Max	Unit
Update rate		44			MSPS
Bandwidth of the output buffer	-3dB	39	53		MHz
Output noise	Fout < 9.9 MHz		0.5		µV/sqrt(Hz)
Wake up time	Sleep to On to first conversion time		2		µs
Power On Time	Pwr Dwn to first conversion time		6		µs

AC LINEARITY

Parameter	Conditions	Min	Typ	Max	Unit
Spurious Free Dynamic Range (SFDR)	Analog Output @ -18dBFS; Fout= 1 MHz		68		dBc
	Analog Output @ 0dBFS Fclk=40MHz; Fout= 9.9 MHz		60		dBc
Total Harmonic Distortion (T.H.D.)	Fclk=40MHz; Fout=9.9MHz; 1Vpp		56		dBc
Channel Isolation		58	60		dBc

This page has been left intentionally blank.

Section: 9 Thermal Characteristics

9.1 Thermal Resistance

Table 105: Thermal Resistance

Θ_{JA} still air (Typ)	Θ_{JA} 1 m/s (Typ)	Θ_{JA} 2.5 m/s (Typ)
26	24	22
With Drop in Heat Spreader		
Θ_{JA} still air (Typ)	Θ_{JA} 1 m/s (Typ)	Θ_{JA} 2.5 m/s (Typ)
16	14	12

Symbol	Definition	Units
Θ_{JA}	Junction-to-ambient thermal resistance – $\Theta_{JA} = (T_J-T_A) / Pd$ Junction-to-air thermal resistance measures the ability of a device to dissipate heat from the surface of the die to the ambient via all paths. This value is to be used for packages without external heat spreaders and similar PCB as JEDEC test board.	°C/Watt
Θ_{JC}	Junction-to-case thermal resistance – $\Theta_{JC} = (T_J-T_C) / Pd$ Junction-to-case thermal resistance measures the ability of a device to dissipate heat from the surface of the die to the top or bottom surface of the package This value is to be used for packages with external heat spreaders and only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.	°C/Watt
T_J	Junction temperature – maximum temperature on the die	°C
T_A	Ambient temperature	°C
T_C	Temperature at the hottest spot of the package	°C
Pd	Total power dissipated from the die to the case	Watt

This page has been left intentionally blank.

Section: 10 Mechanical Specifications

The following mechanical specifications may vary from different manufacturing lots. For more accurate and precise values, Wavesat recommends that a package from each lot be measured again.

Table 106: Mechanical Specifications

Name Body Package	Size (mm)	Thickness (mm)	Outer Lead Pitch (mm)
Plastic Quad Flat Pack (PQFP) 208	28	3.37	0.5

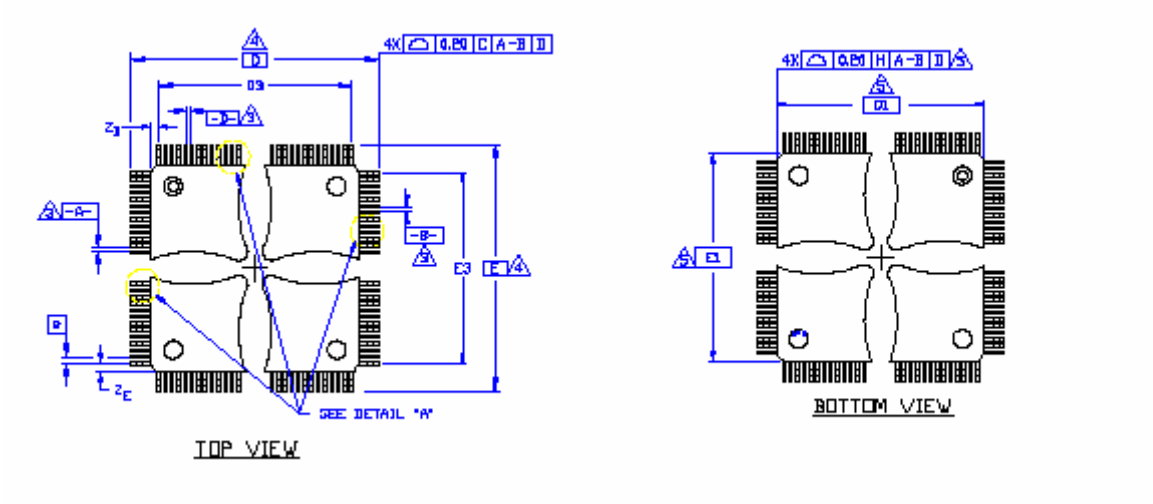


Figure 40: DM 256 Mechanical Design Diagram – Top and Bottom Views

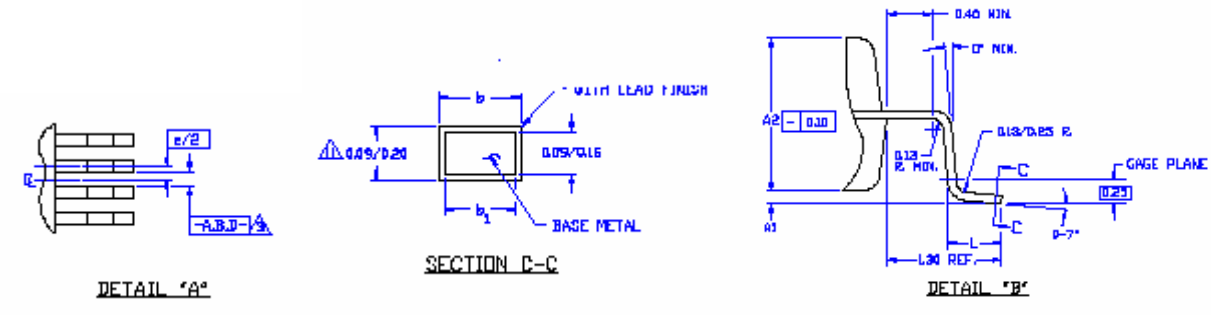


Figure 41: DM 256 Mechanical Design Diagram Details

Table 107: Mechanical Design Detail Measurements

Notes	Symbols	Dimensions (in millimeters)		
		Minimum	Nominal	Maximum
	A		3.70	4.07
	A_1	0.25	0.33	
	A_2	3.309	3.37	3.60
4	**D**	30.60 BSC.		
5	**D_1**	28.00 BSC		
	D_3	25.50 BSC		
	Z_D	1.25 REF		
4	**E**	30.60 BSC		
5	**E_1**	28.00 BSC		
	E_3	25.50 REFC		
	Z_E	1.25 REF		
	L	0.50	0.60	0.75
6	**N**	208		
	e	0.50 BSC		
	b	0.17	0.22	0.27
	b_j	0.17	0.20	0.23
	ddd	0.08		

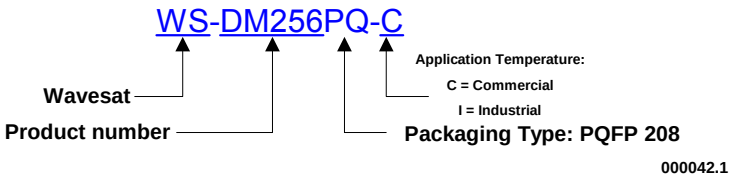
Note:

1. All dimensions and tolerances conform to ANSI Y14.5-1982.
2. Datum plane –H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined where centerline between leads exits plastic body at datum plane –H-
4. To be determined at seating plane –C-
5. Dimensions D_1 and E_1 do not include mold protrusion. Allowable mold protrusion is 0.254 mm per side. Dimension D_1 and E_1 do include mold mismatch and are determined at datum plane –H-
6. N is the total number of terminals
7. Package top dimensions are smaller than bottom dimension by 0.22 mm and top of package will not overhang bottom of package.
8. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition dambar cannot e located on the lower radius or the foot.
9. All dimensions are in millimeters.
10. This drawing conforms to JEDEC registered outline JEDEC MO-143.
11. These dimensions apply to the flat section of the lead between 0.11 mm and 0.25 mm from the lead tip.
12. Maximum allowable die thickness to be assembled in this package family is 0.635 mm.

Section: 11 Ordering Information

Table 108: DM256 IEEE 802.16-2004 OFDM PHY Ordering Information

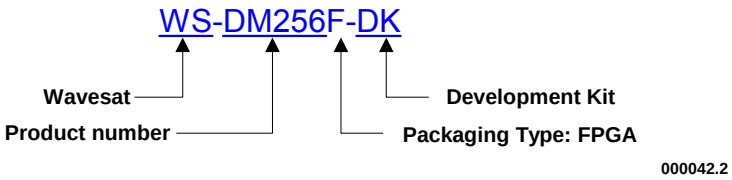
Description	Part Number
DM256 IEEE 802.16-2004 OFDM PHY Commercial Temperature 0 °C to 70 °C	WS-DM256PQ-C
DM256 IEEE 802.16-2004 OFDM PHY Industrial Temperature -40 °C to 85 °C	WS-DM256PQ-I



Note:	Other application temperatures are potentially available on demand. Please contact Wavesat for more information.

Table 109: DM256 Development Kit Ordering Information

Description	Part Number
DM256 Development Kit with Documentation: Development Guide and Data Book	WS-DM256F-DK



For more information:
sales@wavesat.com
support@wavesat.com

Wavesat Inc.
1375 Trans-Canada Highway
Suite 300
Dorval, Quebec H9P 2W8
Canada
(888) 802-1616
(514) 684-0200
Fax: (514) 684-0211
www.wavesat.com

Section: 12 List of Terms and Definitions

ADC	Analog to Digital Converter
AFC	Automatic Frequency Correction
AGC	Automatic Gain Control
ALC	Automatic Level Control
ALU	Arithmetic Logic Unit
ARQ	Automatic Repeat Request
BR	Bandwidth Request
Baseband	Baseband is the original band of frequencies produced by a transducer or any other signal initiating device, prior to initial modulation. Bandwidth is centered at DC (IF freq = 0 Hz)
Base Station (BS)	The equipment that provides connectivity, management, and control of the Subscriber Station (SS).
BER	Bit Error Rate
BPSK	Binary Phase Shift Keying
Broadband	Having instantaneous bandwidths greater than around 1 MHz and supporting data rates greater than about 1.5 Mb/s.
Broadband Wireless Access (BWA)	Wireless access in which the connection(s) capabilities are broadband.
Burst Profile	Set of parameters that describe the uplink or downlink transmission properties associated with an interval usage code. The parameters include symbol type, modulation rate and channel coding.
BW	Bandwidth
Center Frequency	The center of the frequency band in which the transmission occurs. Center frequency of the received or transmitted Bandwidth.
CFG Word	It is the same thing as DL/UL CFG & SCH Frame but is a lot easier to say. Note that "map" may be used synonymously because they are simply different forms of the same thing.
Cheetah	Hardware Medium Access Control layer
CID	Connection Identifier
CINR	Carrier to Interference and Noise Ratio
CMG	Channel Measurement Gap
Connection Identifier CID	A unidirectional MAC address that identifies a connection to equivalent peers in the MAC of the Base Station (BS) and Subscriber Station (SS).
COFDM	Coded Orthogonal Frequency Division Multiplexing
Cyclic Prefix (CP) Size / CP Time	Guard samples per symbol. Possible values are 8, 16, 32 and 64 based on an FFT size of 256 samples per symbol.
CP	Cyclic Prefix
CPE	Customer Premise Equipment as known as Subscriber Station
CRC	Cyclic Redundancy Check
CS	Convergence Sub-layer
DAC	Digital to Analog Converter
DCD	Downlink Channel Descriptor
DFS	Dynamic Frequency Selection
DIUC	Downlink Interval Usage Code
DL	Downlink
DLFP	Downlink Frame Prefix
Downlink (DL)	The direction from the Base Station (BS) to the Subscriber Station (SS).

Downlink Channel Descriptor (DCD)	A MAC message that describes the physical layer characteristics of a downlink channel and is transmitted by the Base Station at a periodic interval.
Downlink Interval Usage Code (DIUC)	An interval usage code used in the downlink. See Interval Usage Code (IUC).
Downlink Map (DL-MAP)	A MAC management message generated at the Base Station and broadcast to all Subscriber Stations. It is software dependent. It describes the burst profiles (configuration and scheduling) of the downlink sub-frame. The DL-MAP is used to create the content of the Rx Frame Configuration Buffer, which is required by each Subscriber Station in order to deconstruct the downlink sub-frame received from the Base Station.
DL-MAP IE	Downlink MAP Information Element
DL/UL CFG & SCH Frame (Descriptor)	It is hardware dependent. It describes the burst profiles (configuration and scheduling) of the downlink sub-frame.
DRAM	Dynamic Random Access Memory
EEPROM	Electronically Erasable Programmable Read-Only Memory
Fast-Fourier Transform (FFT) size	Referred as the “useful” symbol time. The FFT size is the smallest power of two greater than the number of sub-carriers used, which is 200. Therefore, the FFT size is 256 points per symbol.
FCH	Frame Control Header
FDD	Frequency Division Duplex or Duplexing
FEC	Forward Error Correction
FFT	Fast Fourier Transform
FIFO	First In First Out
Frame	A structured set of data that is transmitted over the air interface for a specific duration. DM 256 can be programmed to use the following frame sizes: 2.5, 4, 5, 8, 10, 12.5 and 20 ms. This word can be used synonymously with “Message”.
Frame Descriptor	Information stored in a buffer and that describes the burst profiles (configuration and scheduling) of a frame.
Frequency Division Duplex (FDD)	A duplex scheme in which uplink and downlink transmissions use different frequencies but occur typically at the same time.
FSH	Fragmentation Sub-header
Guard Interval (G)	Ratio of CP Size (a.k.a. CP Time) to FFT size. Possible values are 1/32, 1/16, 1/8 and 1/4.
Half-Duplex Frequency Division Duplex (H-FDD)	A duplex scheme in which uplink and downlink transmissions use not only different frequencies but also occur at different times.
HCS	Header Check Sequence
HEC	Header Error Check
HFDD	Half-Duplex Frequency Duplexing
HSAR	Hardware Segmentation And Re-assembly
HT	Header Type
LOS	Line of Sight
I	In phase
IE	Information Element
IEEE	Institute of Electrical and Electronics Engineers
Interval Usage Code (IUC)	A code identifying a particular burst profile that can be used by a downlink or uplink transmission interval.
IP	Internet Protocol
I/Q	Inphase/Quadrature
IUC	Interval Usage Code
LSB	Least Significant Bit
MAC	Medium Access Control Layer

Message	Describe a group of data, which is a complete entity of varying length, but may be transported over one or more packets. For example: a MAC message may be transported over one or more packets, which may be transmitted over one or more OFDM symbols.
MSB	Most Significant Bit
NFS	Network File System
NLOS	Non Line of Sight
OFDM	Orthogonal Frequency Division Multiplexing
Packet	This word is used to describe a fixed size group of data. This typically refers to a transport packet. 802.16 - 2004 defines many packet sizes depending on modulation and coding rate.
PAPR	Peak to Average Power Ratio
Physical Layer (PHY)	The lowest layer within the OSI Network Model. It deals primarily with transmission of the raw bit stream over the Physical transport medium. In the case of wireless transmission, the transport medium is free space. This layer defines parameters such as data rates, modulation method, signaling parameters, transmitter/receiver synchronization etc. Within an actual radio implementation, the PHY corresponds to the radio front end and baseband signal processing sections.
PMP	Point-to-MultiPoint
PQFP	Plastic Quad Flat Pack
Q	Quadrature
QAM	Quadrature Amplitude Modulation
QoS	Quality of Service
QPSK	Quadrature Phase-Shift Keying
Protocol Data Unit (PDU)	This is a group of data strictly defined by the protocol. It is a formatted group of data exchanged between two adjacent layers of the OSI protocol. In the downward direction, it is the data to be transmitted to the lower layer. On the upward direction, it is the data received from the lower layer. For example, the PHY PDU is the formatted burst of data transmitted over the air.
Receive/Transmit Transition Gap (RTG)	A time interval between the uplink sub-frame and the following downlink sub-frame in time division duplexing (TDD). This time interval allows the Base Station (BS) to switch from receive to transmit mode and Subscriber Stations (SS) to switch from transmit to receive mode. During this time interval, the BS and SS are not transmitting modulated data but simply allowing the BS transmitter carrier to ramp up, the transmit/receive (Tx/Rx) antenna switch to actuate, and the SS receiver section to activate. RTG is not applicable to frequency division duplexing (FDD).
REQ	Request
RF Center Frequency	The center of the frequency band in which a base station (BS) or SS is intended to transmit.
RID	Rate ID
RNG-RSP	Ranging -Response
RS	Reed–Solomon
RTG	Receive/Transmit Transition Gap
Rx	Receiver
Sampling Frequency	The Sampling Frequency is calculated as the product of the nominal channel bandwidth and a sampling factor of 8/7.
SAR	Segmentation And Re-assembly
SDRAM	Synchronous Dynamic Random Access Memory
SERDES	Serialize/De-Serialize
Service Data Unit (SDU)	A formatted group of data exchanged between two adjacent layers of the OSI protocol. In the downward direction, it is the data received from the higher layer. In the upward direction, it is the data to be transmitted to the higher layer.
SMAC	Software Medium Access Control Layer
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface

SSAR	Software Segmentation And Re-assembly
Subscriber Station (SS)	A generalized equipment set providing connectivity between subscriber equipment and a Base Station (BS).
SUI Channel Models	Stanford University Interim Channel Models
Symbol	Describe a coded, modulated group of data, usually for transmission or reception. This typically refers to an OFDM symbol. For example: REF symbol, FCH symbol, DATA symbol, etc.
Symbol Length	Number of samples in a symbol. It is the sum of FFT size and CP Size. Possible values are 264, 272, 288 and 320.
Symbol Time	The Symbol Time is the number of samples in a symbol (Symbol Length) divided by the Sampling Frequency.
Time Division Duplex or Duplexing (TDD)	A duplex scheme where uplink and downlink transmissions occur at different times but may share the same frequency.
Time Division Multiplexing (TDM) Burst	A contiguous portion of a TDM data stream using PHY parameters, determined by the Downlink Interval Usage Code (DIUC), that remain constant for the duration of the burst. TDM bursts are not separated by gaps or preambles.
Time Division Multiple Access (TDMA) Burst	A contiguous portion of the uplink or downlink using PHY parameters, determined by the Downlink Interval Usage Code (DIUC) or Uplink Interval Usage Code (UIUC), that remain constant for the duration of the burst. TDMA bursts are separated by preambles and are separated by gaps in transmission if subsequent bursts are from different transmitters.
Type/Length/Value (TLV)	A formatting scheme that adds a tag to each transmitted parameter containing the parameter type (and implicitly its encoding rules) and the length of the encoded parameter.
TO	Transmission Opportunity
Transmit/Receive Transition Gap (TTG)	A time interval between the downlink sub-frame and the following uplink sub-frame in time division duplexing (TDD). This time interval allows the Base Station (BS) to switch from transmit to receive mode and subscriber stations (SS) to switch from receive to transmit mode. During this time interval, the BS and SS are not transmitting modulated data but simply allowing the BS transmitter carrier to ramp down, the transmit/receive (Tx/Rx) antenna switch to actuate, and the BS receiver section to activate. TTG is not applicable to frequency division duplexing (FDD).
Tx	Transmitter
Uplink (UL)	The direction from a Subscriber Station to the Base Station (BS).
Uplink Channel Descriptor (UCD)	A MAC management message that describes the physical layer characteristics of an uplink channel and is transmitted by the Base Station at a periodic interval.
Uplink Interval Usage Code (UIUC)	An interval usage code used in the uplink. See Interval Usage Code (IUC).
Uplink Map (UL-MAP)	A MAC management message generated at the Base Station and broadcast to all Subscriber Stations. It describes the burst profiles (configuration and scheduling) of the uplink sub-frame. The UL-MAP is used to create the content of the Tx Frame Configuration Buffer which is required by each Subscriber Station in order to construct the uplink sub-frame to be transmitted to the Base Station. A set of information that defines the entire access for a scheduling interval.
UL-MAP IE	Uplink MAP Information Element

www.wavesat.com